Service Manual

Tektronix

HFS 9003
Stimulus System

070-8564-02

Warning
The servicing instructions are for use by qualified personnel only. To avoi personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

Injury Precautions

Use Proper Power Cord To avoid fire hazard, use only the power cord specified for this product.

Avoid Electric Overload To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Ground the Product This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in Explosive Atmosphere To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Use Proper Power Source Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:

DANGER High Voltage

Protective Ground (Earth) Terminal

ATTENTION Refer to Manual

Double Insulated

Certifications and Compliances

CSA Certified Power Cords

CSA Certification includes the products and power cords appropriate for use in the North America power network. All other power cords supplied are approved for the country of use.

Compliances

Consult the product specifications for IEC Installation Category, Pollution Degree, and Safety Class.

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This Service Manual provides you with limited service information for the HFS 9003 Stimulus System.

- The *Specifications* section contains all nominal, typical, and specified characteristics.
- The *Operating Information* section teaches you about each of the front panel controls and how to input simple settings for basic operation.
- The *Theory of Operation* section helps you understand the operation of each of the replaceable modules in the HFS 9003.
- The *Performance Verification* section gives you procedures on how to verify the specified performance of the instrument.
- The *Adjustment Procedures* section lists the adjustments you can make to the instrument.
- The *Maintenance* section instructs you on how to perform general preventive maintenance on the instrument. This section also describes removal, replacement and troubleshooting procedures.
- The *Options* section lists the options available from the factory. This section also describes the procedure for installing field updates to the internal programmed code of the instrument.
- The *Diagrams* section describes and illustrates the major electrical sections of the HFS 9003.
- The *Mechanical Parts List* section lists all of the replaceable parts and describes how to order these parts.

Notation Conventions

The following conventions are used in this manual:

- Signal names are printed in bold capital letters; for example, **SENSE IN**.
- A signal active in the low state is shown with a tilde (~) in front of the signal name; for example, **~ACFAIL**.
- Labels of front panel buttons and connectors are shown in bold capital letters; for example, **ENTER**.
- Labels of menu items are shown in mixed case bold text; for example, the Pulse menu **Amplitude** item.

Related Manuals

Refer to the *HFS 9000 User Manual* (070-8365-01) for additional operating information.

Specifications

The HFS 9000 family of high-speed logic signal source instruments have a modular architecture with factory-configurable cards. The channels are digitally synthesized from a common clock resulting in highly accurate independent placement of rising and falling edges. The instruments are optimized for digital device characterization with unique triggering capabilities and a variety of pulse outputs. The product family also features low RMS jitter, the ability to compensate for external cable skews, and an easy-to-use graphical human interface.

This section contains the complete specifications for the HFS 9000 Stimulus System and Modules. These specifications are classified as either nominal traits, warranted characteristics, or typical characteristics.

Nominal Traits

Nominal traits are described using simple statements of fact such as "+2.6 V" for the trait "Maximum high level," rather than in terms of limits that are performance requirements.

Table 1–1: Nominal Traits — HFS 9PG1 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+2.6 V
Minimum low level	–2.00 V
Maximum amplitude	3.00 V
Minimum amplitude	0.50 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to –2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than –2 V may cause malfunction. Level accuracy specifications do not apply when terminating to –2 V. Both true and complement outputs must be terminated to the same voltage.

Table 1–1: Nominal Traits — HFS 9PG1 Output Performance (Cont.)

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1–2: Nominal Traits — HFS 9PG2 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.50 V
Minimum low level	–2.00 V
Maximum amplitude	5.50 V
Minimum amplitude	0.50 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to –2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than –2 V may cause malfunction. Level accuracy specifications do not apply when terminating to –2 V. Both true and complement outputs must be terminated to the same voltage.
Transition time 20% to 80%	Variable from 800 ps to 5 ns
Transition time resolution	10 ps
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1–3: Nominal Traits — HFS 9DG1 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.0 V
Minimum low level	–2.5 V
Maximum amplitude	3.00 V
Minimum amplitude	0.01 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to –2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than –2 V may cause malfunction. Level accuracy specifications do not apply when terminating to –2 V. Both true and complement outputs must be terminated to the same voltage.
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1–4: Nominal Traits — HFS 9DG2 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.50 V
Minimum low level	–2.00 V
Maximum amplitude	5.50 V
Minimum amplitude	0.01 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to –2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than –2 V may cause malfunction. Level accuracy specifications do not apply when terminating to –2 V. Both true and complement outputs must be terminated to the same voltage.
Transition time 20% to 80%	Variable from 800 ps to 6 ns

Table 1–4: Nominal Traits — HFS 9DG2 Output Performance (Cont.)

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Transition time resolution	10 ps
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1–5: Nominal Traits — Time Base

Name	Description
Frequency range	HFS 9PG1, HFS 9DG1: 50 kHz to 630 MHz HFS 9PG2, HFS 9DG2: 50 kHz to 300 MHz[1]
Frequency resolution	≤ 0.1% of frequency setting
Minimum frequency setting when using half, quarter, or eighth pulse rate modes[2]	half pulse rate: 100 kHz quarter pulse rate: 200 kHz eighth pulse rate: 400 kHz
Number of pulse periods in burst or auto-burst modes	User selectable from 1 to 65,536

[1] **If the HFS 9PG2 or HFS 9DG2 is operated in half pulse rate mode, frequency can be extended to 600 MHz for the HFS 9PG2 and 630 MHz for the HFS 9DG2.**

[2] **All pulse rate modes result in 50 kHz output frequency.**

Table 1–6: Nominal Traits — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN input characteristic	0.1 μF DC blocking capacitor followed by 50 Ω termination to ground
Phase lock output frequency range	Any 2^n multiple or sub-multiple of the phase lock frequency that is within the allowed frequency range for the card being used
FRAME SYNC IN	Initiates a burst when using phase lock mode
FRAME SYNC IN input characteristic	50 Ω terminated to –2 V

Table 1–7: Nominal Traits — Output Edge Placement Performance[1]

Name	Description
Channel deskew (**Chan Delay**) range, channels relative to time zero reference	–60 ns to 2.0 µs
Channel deskew (**Chan Delay**) resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Delay (**Lead Delay**) adjustment range	Zero to 20 µs
Delay (**Lead Delay**, **Trail Delay**) adjustment resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Pulse width adjustment range	HFS 9PG1, HFS 9PG2: Zero to (one period – 790 ps) inclusive HFS 9DG1, HFS 9DG2: Zero to (one period × 65,536) inclusive
Pulse width adjustment resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Fine knob resolution of timing	5 ps

[1] **Measured at 50% levels, each channel independent.**

Table 1–8: Nominal Traits — Transducer In Performance

Name	Description
TRANSDUCER IN input characteristic	HFS 9PG1: 1000 pF DC blocking capacitor followed by 50 Ω termination to ground HFS 9PG2: 100 pF DC blocking capacitor followed by 50 Ω termination to ground

Table 1–9: Nominal Traits — Skew Cal In Performance

Name	Description
SKEW CAL IN usage	Calibration use only. No signal, except from a channel **OUTPUT** connector during the calibration process, should ever be applied to this input.

Table 1–10: Nominal Traits — Trigger In Performance

Name	Description
Input Voltage range	±5 V maximum
Trigger level range	±4.70 V
Trigger level resolution	100 mV

Table 1–11: Nominal Traits — Trigger Out Performance

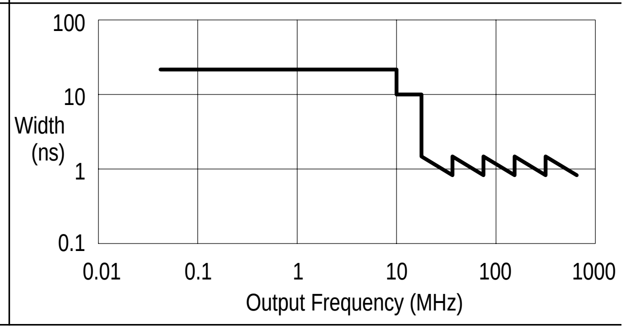
Name	Description
Pretrigger range, **TRIGGER OUT** before time zero reference	Zero to 70 ns
TRIGGER OUT pulse width in auto mode	

Table 1–12: Nominal Traits — Power Requirements

Name	HFS 9003 Description	HFS 9009 Description
Fuse ratings	5 A, 250 V, type 3AG, (Tektronix part 159-0014-00), and 4 A, 250 V, type 3AG, fast blow, (Tektronix part 159-0017-00)	15 A, 250 V, type 3AG, fast blow, (Tektronix part 159-0256-00)

Table 1–13: Nominal Traits — System Memory Performance

Name	Description
Non-volatile memory retention time	Instrument settings and calibration constants are retained in non-volatile memory for 5 years or more. Card identification is retained for 10 years. Extended storage above 50° C may degrade the life of all non-volatile memory.

Table 1–14: Nominal Traits — HFS 9003 Mechanical

Name	Description		
Weight, in 12-channel configuration. (Shipping weight includes all standard accessories.)		Cabinet	Rackmount
	Net weight:	45 lbs. (20.5 kg)	51 lbs. (23.2 kg)
	Shipping weight:	60 lbs. (27.3 kg)	66 lbs. (30.0 kg)
Overall Dimensions		Cabinet	Rackmount
	Width:	16.3 in. (414 mm)	19.0 in (483 mm)
	Height:	7.0 in. (178 mm)	7.0 in. (178 mm)
	Depth:	24.75 in. (629 mm)	24.75 in. (629 mm)
	Depth behind rack flange:	—	22.0 in. (559 mm)
Cooling Method	Forced-air circulation with no air filter, maximum 318 cfm		
Construction Material	Chassis parts are constructed of aluminum alloy; bezel is glass-filled polycarbonate with Lexan plastic inserts; cabinet is aluminum with textured epoxy paint.		

Table 1–15: Nominal Traits — HFS 9009 Mechanical

Name	Description	
Weight, in 36-channel configuration. (Shipping weight includes all standard accessories.)		Rackmount
	Net weight:	81 lbs. (33.7 kg)
	Shipping weight:	100 lbs. (45.3 kg)
Overall Dimensions		Rackmount
	Width:	16.75 in (425.79 mm)
	Height:	14.00 in. (355.89 mm)
	Depth:	24.00 in. (610.11 mm)
Cooling Method, mainframe	Forced-air circulation with air filter, maximum 318 cfm	
Cooling Method, power supply	Forced-air circulation, maximum 106 cfm	
Construction Material	Chassis parts are constructed of aluminum alloy with Lexan plastic inserts; cabinet is aluminum with textured epoxy paint.	

Warranted Characteristics

Warranted characteristics are described in terms of quantifiable performance limits which are warranted. Names of characteristics that appear in boldface type have checks for verifying the specifications in the *Check Procedures* section.

Table 1–16: Warranted Characteristics — HFS 9PG1 Output Performance

Name	Description
High level accuracy (amplitude ≥ 1 V or high level ≥ 0 V)[1]	±2% of level, ±50 mV
Low level accuracy (amplitude ≥ 1 V or high level ≥ 0 V)[1]	±2% of high level, ±2% of amplitude, ±50 mV
Transition time 20% to 80% (amplitude ≤ 1 V)	≤ 200 ps

[1] **If amplitude < 1 V and high level < 0 V, accuracy typically meets the specification but is not guaranteed**

Table 1–17: Warranted Characteristics — HFS 9PG2 Output Performance

Name	Description
High level accuracy	±2% of level, ±50 mV
Low level accuracy	±2% of high level, ±2% of amplitude, ±50 mV
Transition time accuracy 20% to 80% (amplitude ≤ 1 V)	±10% of setting, ±300 ps

Table 1–18: Warranted Characteristics — HFS 9DG1 Output Performance

Name	Description
High level accuracy (amplitude ≥ 0.5 V)[1]	±2% of level, ±50 mV
Low level accuracy (amplitude ≥ 0.5 V)[1]	±2% of high level, ±2% of amplitude, ±50 mV
Transition time 20% to 80% (amplitude ≤ 1 V)	≤ 250 ps

[1] **If amplitude < 0.5 V, accuracy typically meets the specification but is not guaranteed**

Table 1–19: Warranted Characteristics — HFS 9DG2 Output Performance

Name	Description
High level accuracy (amplitude ≥ 0.5 V)[1]	±2% of level, ±50 mV
Low level accuracy (amplitude ≥ 0.5 V)[1]	±2% of high level, ±2% of amplitude, ±50 mV
Transition time accuracy 20% to 80% (amplitude ≤ 1 V)	±10% of setting, ±300 ps

1 **If amplitude < 0.5 V, accuracy typically meets the specification but is not guaranteed.**

Table 1–20: Warranted Characteristics — Time Base

Name	Description
Frequency accuracy	±1%

Table 1–21: Warranted Characteristic — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN frequency range	6 MHz to 630 MHz

Table 1–22: Warranted Characteristics — Output Edge Placement Performance[1]

Name	Description
Delay of pulses relative to time zero reference (Lead Delay) accuracy	HFS 9PG1, HFS 9PG2: 1% of (**Lead Delay** + **Chan Delay**) ±300 ps HFS 9DG1, HFS 9DG2: 1% of (**Lead Delay** + **Chan Delay**) ±50 ps
Pulse width accuracy	HFS 9PG1: 1% of width ±300 ps HFS 9PG2: 1% of width ±300 ps [for widths ≥ 20 ns]; 1% of width + 300 ps, –500 ps [for widths < 20 ns] HFS 9DG1: 1% of width +50 –75 ps HFS 9DG2: 1% of width + 50 ps, –250 ps [for widths ≥ 20 ns]; 1% of width + 50 ps, –450 ps [for widths < 20 ns]

1 **Measured at 50% levels, each channel independent.**

Table 1–23: Warranted Characteristics — Trigger Out Performance

Name	Description
TRIGGER OUT signal levels	Amplitude ≥ 300 mV (–0.5 V ≥ offset ≥ –1.5 V, driving 50 Ω to ground)

Table 1–24: Warranted Characteristics — Power Requirements

Name	Description
Primary circuit dielectric breakdown voltage	1500 VAC_{RMS}, 60 Hz for 10 seconds without breakdown
Primary Grounding	0.1 Ω maximum from chassis ground and protective earth ground

Table 1–25: Warranted Characteristics — Environmental and Safety

Name	HFS 9003 Description	HFS 9009 Description
Temperature	Operating: 0° C to +50° C (32° F to 122° F) Non-operating (storage): –40° C to +75° C (–40° F to 167° F)	Operating: 0° C to +40° C (32° F to 104° F) Non-operating (storage): –40° C to +75° C (–40° F to 167° F)
Altitude	Operating: 4 hours at 3,048 m (10,000 feet). Derate maximum operating temperature by –1° C (–1.8° F) for each 304.8 m (1,000 feet) above 1,524 m (5,000 feet) Non-operating: 2 hours at 12,192 m (40,000 feet)	
Humidity	Operating: < 95% RH, non-condensing, from 0° C to 30° C (32° F to 86° F) < 75% RH, non-condensing, from 31° C to 40° C (88° F to 104° F) (MIL-T-28800E, para 4.5.5.1.2.2, Type III, Class 5)	
Shock (non-operating)	MIL-T-28800E, para 4.5.5.4.1, Type III, Class 5	
Resistance to mishandling during bench use (operating)	MIL-T-28800E, para 4.5.5.4.3, Type III, Class 5	
Resistance to packaged transportation vibration, sinusoidal, in shipping package	Drops of 36 inches on all edges, faces, and corners National Safe Transit Association, test procedure 1A-B-2	
Resistance to packaged transportation vibration, sinusoidal, in shipping package	Packaged sinusoidal vibration National Safe Transit Association, test procedure 1A-B-1	
Resistance to packaged transportation random vibration	MIL-STD-810D, method 514.3, category I, Figure 514.3-1	

Table 1–25: Warranted Characteristics — Environmental and Safety (Cont.)

Name	HFS 9003 Description	HFS 9009 Description
Safety	Listed to UL1244 Certified to CAN/CSA-C22.2 No. 231–M89	
IEC Specifications	Installation Category II Pollution Degree 2 Safety Class I	

Typical Characteristics

Typical characteristics are described in terms of typical or average performance. Typical characteristics are not warranted.

Table 1–26: Typical Characteristics — Time Base

Name	Description
RMS jitter	15 ps, ±0.05% of interval
Recovery time between bursts or auto-bursts	15 μs

Table 1–27: Typical Characteristics — HFS 9PG1 Output Performance

Name	Description
Transition time 20% to 80%	Amplitude ≤ 1 V: 150 ps 1 V < Amplitude ≤ 2 V: 190 ps 2 V < Amplitude ≤ 3 V: 225 ps
Output aberrations (beginning 200 ps after 50% point of transition)	Overshoot: +15%, +20 mV Undershoot: –10%, –20 mV

Table 1–28: Typical Characteristics — HFS 9PG2 Output Performance

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Transition time accuracy 20% to 80%	±10% of setting, ±300 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: –10%, –20 mV

Table 1–29: Typical Characteristics — HFS 9DG1 Output Performance

Name	Description
Transition time 20% to 80%	Amplitude ≤ 1 V: ≤ 250 ps, 250 ps 1 V < Amplitude < 2 V: 250 ps 2 V ≤ Amplitude ≤ 3 V: 260 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: –10%, –20 mV

Table 1–30: Typical Characteristics — HFS 9DG2 Output Performance

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Transition time accuracy 20% to 80%	±10% of setting, ±300 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: –10%, –20 mV

Table 1–31: Typical Characteristics — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN amplitude range	0.8 V to 1.0 V peak-to-peak
PHASE LOCK IN transition time requirement	20% to 80% in ≤ 10 ns
FRAME SYNC IN signal level	$-1.810\ V \leq V_{low} \leq -1.475\ V$ $-1.165\ V \leq V_{high} \leq -0.810\ V$ (standard 100 K ECL levels)
Setup time, rising edge of **FRAME SYNC IN** signal to rising edge of **PHASE LOCK IN**	650 ps minimum
Hold time, high level of **FRAME SYNC IN** after rising edge of **PHASE LOCK IN**	650 ps minimum
Time from frame sync qualified phase lock clock cycle to time-zero reference	70 ns minimum, 130 ns

Table 1–32: Typical Characteristics — Transducer In Performance

Name	Description
TRANSDUCER IN useful frequency range	HFS 9PG1: 25 MHz to > 1 GHz HFS 9PG2: 5 MHz to 300 MHz
TRANSDUCER IN amplitude requirement	1.0 V to 1.5 V peak-to-peak

Table 1–33: Typical Characteristics — Trigger In Performance

Name	Description
Input resistance	50 Ω
Trigger level accuracy	±100 mV ±5% of trigger level
Trigger input rise/fall time requirement	≤ 10 ns
Minimum trigger input pulse width	1 ns
Trigger sensitivity	≤ 500 mV
Time from trigger in to time-zero reference	70 ns minimum, 130 ns typical

Table 1–34: Typical Characteristics — Trigger Out Performance

Name	Description
Pretrigger resolution	250 ps

Table 1–35: Typical Characteristics — Power Requirements

Name	HFS 9003 Description	HFS 9009 Description
Line Voltage	90 VAC_{RMS} to 130 VAC_{RMS} or 180 VAC_{RMS} to 250 VAC_{RMS}, range switched automatically	90 VAC_{RMS} to 104 VAC_{RMS} with maximum 7 cards installed, 104 VAC_{RMS} to 132 VAC_{RMS} with maximum 9 cards installed, or 180 VAC_{RMS} to 250 VAC_{RMS}, range switched automatically
Line frequency	48 Hz to 63 Hz	
Power consumption	540 W maximum	1190 W with maximum of 9 cards installed
Inrush surge current	50 A maximum up to 40 ms at 110 VAC 100 A maximum up to 40 ms at 220 VAC	

Operating Information

The HFS 9003 is built in a portable C-size VXIbus card-modular mainframe (see Figure 2–1). It has a CPU card, a time base card, and up to three pulse or data generator cards. A front panel module provides a keyboard and a gas-discharge flat-panel display.

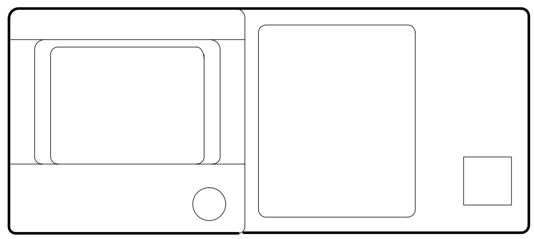


Figure 2–1: HFS 9003 Mainframe and Front Panel

This section shows how to input simple settings for basic operation. For a more thorough explanation of how to set up the instrument, refer to the *HFS 9000 Series User Manual*.

Menu Selections

The front panel **MAIN MENU** button, shown in Figure 2–2, displays the top level menu. Each item in this menu leads to a second-level menu. You can move through all menus using the arrow keys surrounding the **SELECT** button. Each arrow button moves the selection to the next menu item in the direction indicated. When the desired menu item is highlighted, press the **SELECT** button to activate that selection.

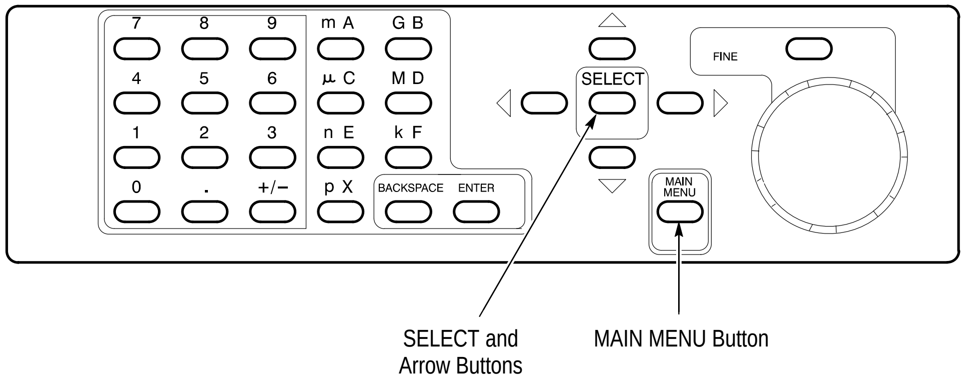


Figure 2–2: MAIN MENU, SELECT, and Arrow Button Locations

Resetting the HFS 9003

To reset all user-selected parameters to known default settings:

1. Press the **MAIN MENU** button (see Figure 2–2).
2. Use the arrow buttons to highlight the **Save/Recall Menu** item in the main menu (see Figures 2–2 and 2–3). Press the **SELECT** button.

Main Menu

press SELECT to show the Pulse Menu.

Pulse Menu	Time Base Menu	Levels Menu	Signal Menu
Vector Menu	Data Edit Menu	Data Fill Menu	Data Copy Menu
Save/Recall Menu	GPIB Menu	RS-232 Menu	Cal/Deskew Menu

Figure 2–3: Main Menu Display

3. Highlight the **Reset** item and press **SELECT** again.
4. Verify the reset selection by highlighting the **Yes** in the subsequent dialog box, then press **SELECT**. (To select options in the dialog box, use the up and down arrow keys, or turn the knob.)

Setting the Time Base

All pulse or data generator channels are governed by a single time base. The following steps set up the time base to self-trigger repeatedly and to specify the number of pulses to be output from the pulse or data generators.

1. Press the **MAIN MENU** button.
2. Highlight the **Time Base Menu** item in the main menu. Press the **SELECT** button.

   The time base normally waits for a trigger event, and then specifies the number of pulses (**Count**) to be generated (see Figure 2–4). After that, the time base pauses for a rearm time, and then waits for the next trigger event. The display screen above the Time Base menu graphically depicts this sequence.

Time Base Menu

press SELECT: Auto Burst ▶Auto-Burst Trig-Auto

Mode Auto-Burst	Period 1.7ns	Count 1	Out Period 1
Trigger In On	Trig Slope Positive	Trig Level 0V	PhaseLockIn Off
Run/Stop Running	—	—	—

Figure 2–4: The Time Base Menu

3. Use the arrow keys to highlight the **Mode** item. Press the **SELECT** button twice to select **Auto-Burst** in the menu item (see Figure 2–5).

Time Base Menu

press SELECT: Auto Burst ▶Auto-Burst Trig-Auto

Mode Auto-Burst

Figure 2–5: Mode set to Auto-Burst

   The **Period** and **Count** settings control the generated pulses. When either of these items are highlighted, the waveform display above the menu is updated to illustrate the parameter being adjusted.

4. Select the **Period** item. Use the knob to adjust the period. To get finer resolution, press the **FINE** button. The **FINE** light illuminates to indicate fine mode is selected.

   You may also enter numeric values with the keypad. Type in the number and, if necessary, press a key to specify units. Then finish by pressing the **ENTER** key.

5. Select the **Count** item. Set a value using the knob, or type a value using the keypad. Press **ENTER** to terminate keypad entry.

   The **Period** item can also be used to specify **Frequency**. When **Period** is highlighted, the **SELECT** button alternates between **Period** and **Frequency**. Use the knob or keypad to set values.

6. Highlight the **Period** item and press the **SELECT** button. Observe that the period setting changes to a reciprocal frequency setting.

The HFS 9003 is now set up to enable the output of pulses. Since the HFS 9003 is in auto-burst mode, no trigger input is required to generate pulses.

The RUN/STOP Button

You can start and stop the time base by pressing the RUN/STOP button on the front panel.

The UNDO Button

Whenever a setting is changed, the HFS 9003 remembers the old setting as well. Pressing the **UNDO** button (located to the right of the display panel) restores the last setting. Pressing it twice undoes the undo.

Pulse Output

The following procedure demonstrates how to switch the pulse generator channels on. Any channel can be turned on from the Pulse menu **Output** item, but it is more convenient to turn on a channel from the front panel. Depending on the configuration of the HFS 9003, there are one, two, or three pulse or data generator cards, each with up to four channels. The controls for each type of card are shown in Figure 2–6.

1. Select a channel to use for the output by pressing the **OUTPUT** button for that channel. Observe that the associated light illuminates. If you want to use $\overline{\textbf{OUTPUT}}$ for any generator channel, you must turn on the $\overline{\textbf{OUTPUT}}$ separately.

The HFS 9003 is now creating pulse bursts. It generates the number of pulses entered for the count value at the frequency entered for the corresponding period value (or frequency value). When the pulse train is completed, it automatically starts over again after the rearm time.

2. Connect a cable to the output to access the generated pulses.

3. To achieve normal burst mode operation, highlight the **Mode** item of the Time Base menu. Use the **SELECT** button to select **Burst** mode. If burst is selected, the output is no longer triggered (unless a suitable trigger signal is applied to the time base card **TRIGGER IN** connector). Press the **MANUAL TRIGGER** button (to the right of the display panel) to initiate a single burst from the HFS 9003.

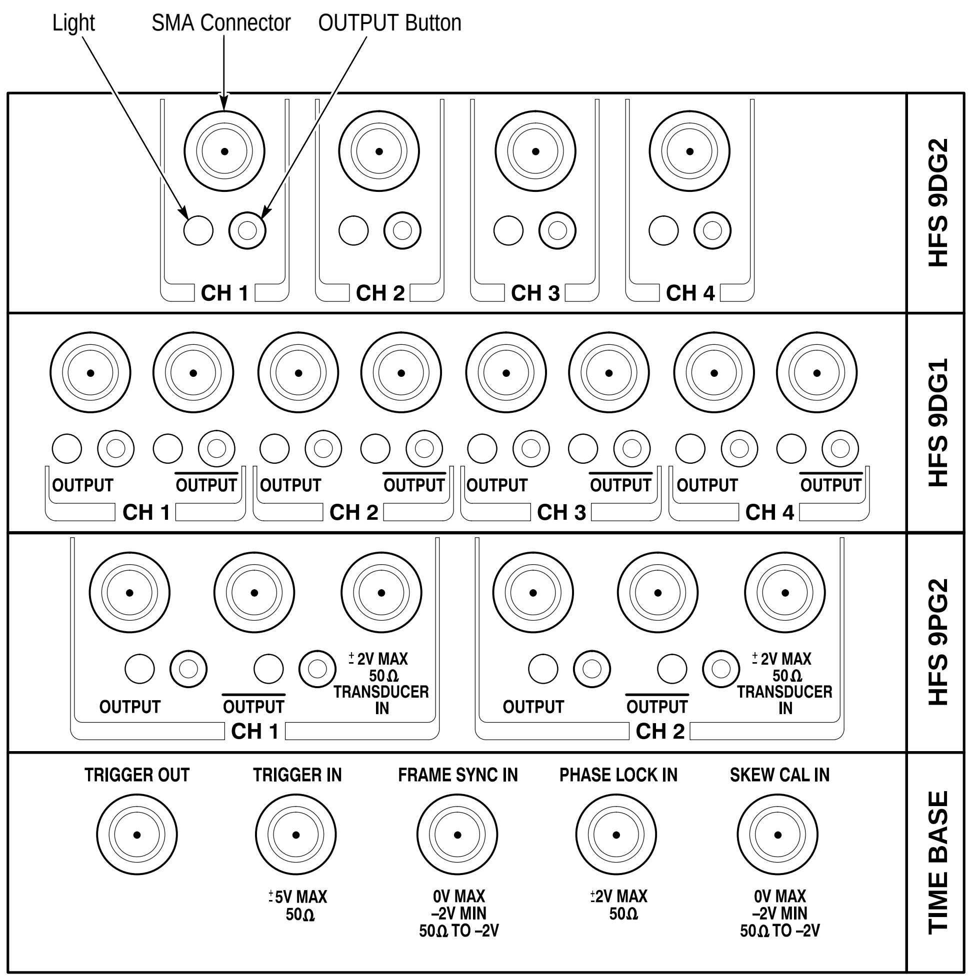


Figure 2–6: Controls and Connectors for the Pulse, Data Time Generator, and Time Base Cards

Strap Settings

The only strap or jumper settings in the HFS 9003 are on the backplane. Figure 3–1 shows the proper setting of these jumpers.

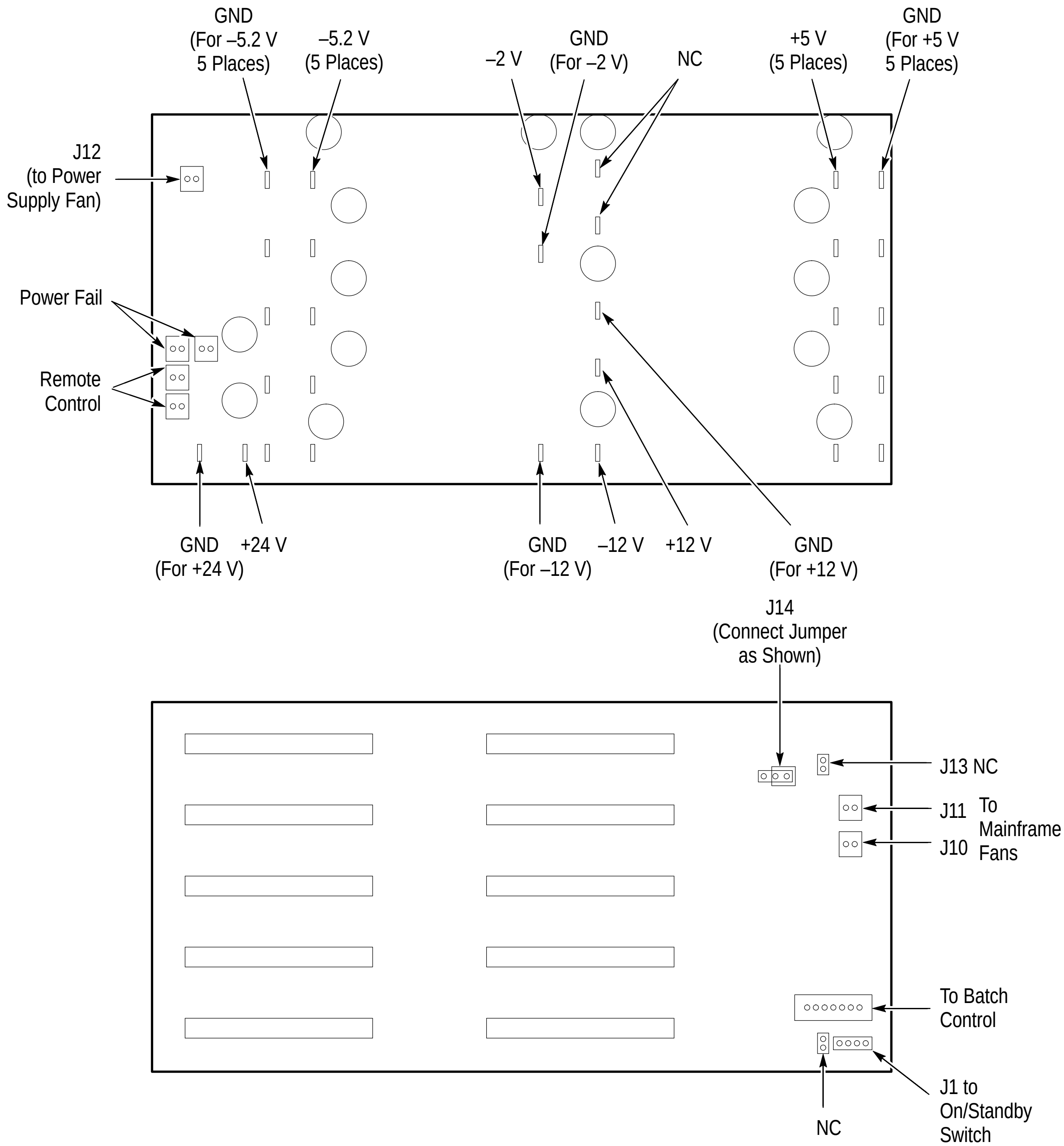


Figure 3–1: Backplane Jumper Settings and Connections

Module Descriptions

This section describes the operation of each of the replaceable modules in the HFS 9003 Stimulus System. Refer to the *Diagrams* section of this manual for a block diagram of the HFS 9003.

Mainframe

The mainframe consists of a backplane, two power supplies, and three fans.

Backplane

The backplane complies with the *VXIbus System Specification Rev.1.2*, dated June 21, 1989. The backplane has five slots and is VXIbus standard C size.

Power Supplies

Two interconnected power supply modules are used to provide all the voltages for the HFS 9003. The power supply mounted closest to the front of the instrument provides –5.2 VDC, –2 VDC, and +24 VDC. The power supply mounted closest to the rear provides +5 VDC, +12 VDC, and –12 VDC.

The power supply modules feature automatic line voltage switching and remote switching for the **ON/STANDBY** switch (located on the front panel). The power supplies are serviced as modules; no description of module circuitry is provided.

The **ON/STANDBY** switch is an SPDT latching switch with a replaceable built-in lamp. It is connected to the power supply modules **REMOTE CONTROL** inputs, allowing low voltage, low current switching control.

When the **ON/STANDBY** switch is turned on, the power supply modules **REMOTE CONTROL** line is released from ground, turning on the power supplies. Simultaneously, the **~ACFAIL** signal is also released from ground. As the +5 V rises, **~SYS RESET** is forced low for at least 200 ms, resetting all the VXIbus cards.

When the **ON/STANDBY** switch is turned to standby, the **~ACFAIL** signal is immediately forced low. Approximately 10 ms later, **~SYS RESET** is driven low. The **REMOTE CONTROL** lines go low approximately 30 ms after the power switch is turned to standby, shutting down the power supply modules.

If either power supply module detects an AC line interruption, it pulls the **POWER FAIL** signal low, which immediately forces **~ACFAIL** low. However, the other power supply module may continue to operate if it does not detect the same AC line interruption.

Fans Three fans provide cooling for the power supply modules and the VXIbus modules installed in the card cage. The two forward fans cool the card cage and run at temperature-controlled variable speed. The single fan in the rear of the chassis cools the power supply modules and also runs at a temperature-controlled rate.

The temperature sensor for the fans is located on the left edge of the backplane and monitors the exhaust air temperature. An op amp circuit connected between the temperature sensor and the fan drivers acts as a low pass filter to prevent rapid changes in fan speeds.

All fans draw their power from the +12 V power supply, and draw a total of approximately 1.5 Amps.

Front Panel Module

The front panel module contains a scan push-button matrix and LEDs, and mechanically supports the electroluminescent display.

Cards

Four types of cards plug into the mainframe: the CPU card, the time base card, the pulse generator cards, and the data time generator cards. Each HFS 9003 has one CPU card, one time base card, and a maximum of three pulse or data generator cards.

CPU Card The CPU receives commands for pulse output parameters from the front panel, the GPIB, or RS-232 interfaces. The CPU creates a series of time base and pulse card commands which are then transmitted via the VXI Bus to set up the pulse outputs.

The CPU card contains all product code in read-only memory (ROM). The CPU card also has volatile and nonvolatile random-access memory (RAM), as well as video display and bus timing circuitry.

Time Base Card The time base contains a voltage-controlled oscillator, which is tunable from 325 MHz to 650 MHz. The time base also contains the trigger in, trigger out, and phase lock circuits.

The VCO output is connected to the pulse and data generator cards through clock distribution cables. Clock distribution cables are located at the front of the cards. The time base card provides several connections for clock distribution cables, one of which is connected to each pulse or data generator card. The clock distribution cables provide a high-speed signal path for the clock, because the VXIbus backplane cannot carry signals of sufficiently high frequency.

Pulse Generator Cards

Each pulse generator card provides two independent output channels. Each channel provides standard and logically-complemented outputs.

The pulse generator card channels divide the master clock signal into the requested frequency, and format the output signals. The pulse generator card controls the channel output levels, the channel delay, and the channel rising and falling edge time.

The pulse generator card transducer input can be used to bypass the VCO and timing generation circuits in the HFS 9003. When transducer in is enabled, a sine wave can be applied to the transducer input. You can use the channel output levels and rise and fall times to reshape the input signal.

High Speed Pulse Generator Cards (HFS 9PG1) run at a top speed of 630 MHz and have a fixed rise and fall time of 200 ps.

Variable Rate Pulse Generator Cards (HFS 9PG2) run at a top speed of 300 MHz. The rise time and fall times can be independently programmed from less than one nanosecond to five nanoseconds, which allows the user to adjust the speed of the pulse edges.

Data Time Generator Cards

Each data time generator card provides four independent output channels. The high speed data time generator card provides standard and logically-complemented outputs. The variable rate data time generator card provides only a single output for each channel. The data time generator card channels work in the same way as the pulse generator card channels. The master clock signal is divided into the requested frequency and format output signals by controlling the output levels, channel delay, and rising and falling edge time.

High Speed Data Time Generator Cards (HFS 9DG1) run at a top speed of 630 MHz and have a fixed rise and fall time of 200 ps.

Variable Rate Data Time Generator Cards (HFS 9DG2) run at a top speed of 300 MHz. The rise and fall times can be independently programmed from less than one nanosecond to five nanoseconds, which allows the user to adjust the speed of the pulse edges.

Performance Verification

The following tests verify that the HFS 9000 Stimulus System achieves its specified performance.

Required Test Equipment

Refer to Table 4–1 for a list of the test equipment required to verify performance.

Table 4–1: Required Test Equipment

Item Number and Description		Minimum Requirements	Example	Purpose
1	Digital Volt Meter	DC volt accuracy: ± 0.1% from 0.40 V to 5.5 V	Tektronix DM 511	Output level and amplitude checks
2	BNC female to dual banana plug	—	Tektronix part number 103-0090-00	Output level and amplitude checks
3	Cable, Precision Coaxial, BNC	36-inch, 50 Ω	Tektronix part number 012-0482-00	Output level and amplitude checks
4	Precision Feed-through Terminator	50 Ω, 0.1% at DC	Tektronix part number 011-0129-00	Output level and amplitude checks
5	Digital Sampling Oscilloscope	Δ time accuracy: ± (0.25% + 10 ps) from 100 ps to 1 µs Freq. Measurement accuracy: ± 0.10% from 50 kHz to 630 MHz	Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer	Trigger Output Check, Rise and fall time checks, Edge placement checks, Frequency accuracy check
6	Sampling Head	Rise time: ≤ 60 ps (10% to 90%)	Tektronix SD-22, SD-24, or SD-26	Used with Tektronix Digital Sampling Oscilloscope (item 5)
7	Attenuator, 5X, SMA	50 Ω, ≥ 12 GHz bandwidth	Tektronix part number 015-1002-00	Rise and fall time checks
8	Cable, Coaxial, SMA (two required)	20-inch, 50 Ω	Tektronix part number 174-1427-00	Trigger Output Check, Rise and fall time checks, Edge placement check, Frequency accuracy check
9	Generator, Leveled Sine Wave	Capable of producing 0.8 V_{p-p} amplitude up to 600 MHz into 50 Ω	Tektronix SG 504	Phase lock check

Table 4–1: Required Test Equipment (Cont.)

Item Number and Description	Minimum Requirements	Example	Purpose
10 BNC female to SMA male adapter	—	Tektronix part number 015-1018-00	Output level and amplitude checks, Phase lock check
11 Threaded SMA female to SMA male slip-on connector	—	Tektronix part number 015-0553-00	SMA quick disconnect

Test Record

Identify the type of cards you will be testing and photocopy the appropriate tables from pages 4–3 to 4–9. Use these tables to record the performance test results for the instrument.

Table 4–2: Trigger Output Level and Phase Lock Test

Page ______________________ of ____________________

Instrument Serial Number:	____________________	Certificate Number:	____________________
Temperature:	____________________	RH %:	____________________
Date of Calibration:	____________________	Technician:	____________________

Performance Test			Minimum	Incoming	Outgoing	Maximum
Trigger Output Level Amplitude ≥ 300 mV (–0.5 V ≥ offset ≥ –1.5 V, driving 50 Ω to ground)						
Output	Maximum High Level		N/A	__________	__________	≤ –0.5 V
	Minimum Low Level		≥ –1.5 V	__________	__________	N/A
	Minimum Amplitude		≥ 300 $mV_{p–p}$	__________	__________	N/A
Phase Lock Test 1% (frequency set accuracy of generator)						
Output Channel	0.8 V, 250 MHz 0.8 V, 594 MHz	250 MHz 594 MHz	247.5 588.1	__________ __________	__________ __________	252.5 599.9

Table 4–3: Test Record for HFS 9DG1 Card

Channel: ______	Page ______ of ______
Instrument Serial Number: ______	Certificate Number: ______
Temperature: ______	RH %: ______
Date of Calibration: ______	Technician: ______

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: ± 2% of level, ± 50 mV Low Level: ± 2% of High Level, ± 2% of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+5.0 V	+4.850	______	______	+5.150
	Normal	+2.0 V	1.790	______	______	+2.210
	Normal	–2.5 V	–2.680	______	______	–2.320
	Complement	–1.5 V	–1.580	______	______	–1.420
Not Output Channel	Normal	+5.0 V	+4.850	______	______	+5.150
	Complement	+2.0 V	1.790	______	______	+2.210
	Complement	–2.5 V	–2.680	______	______	–2.320
	Normal	–1.5 V	–1.580	______	______	–1.420
Rise Time / Fall Time ≤ 250 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	250 ps	N/A	______	______	250 ps
	Complement, 1 V, Tf	250 ps	N/A	______	______	250 ps
Not Output Channel	Normal, 1V, Tf	250 ps	N/A	______	______	250 ps
	Complement, 1 V, Tr	250 ps	N/A	______	______	250 ps
Edge Placement Pulse Delay Time 1% of (**Lead Delay** + **Chan Delay**) ±50 ps						
Output Channel	Normal	100 ps	49	______	______	151
		500 ps	445	______	______	555
		1 ns	0.940	______	______	1.060
		5 ns	4.900	______	______	5.100
		10 ns	9.850	______	______	10.150
		50 ns	49.45	______	______	50.55
		100 ns	98.95	______	______	101.05
Not Output Channel	Normal	100 ps	49	______	______	151
		500 ps	445	______	______	555
		1 ns	0.940	______	______	1.060
		5 ns	4.900	______	______	5.100
		10 ns	9.850	______	______	10.150
		50 ns	49.45	______	______	50.55
		100 ns	98.95	______	______	101.05
Edge Placement Pulse Width Variance 1% of width ± 50 ps						
Output Channel	Normal	500 ps	445	______	______	555
		750 ps	693	______	______	808
		1 ns	0.940	______	______	1.060
Not Output Channel	Normal	500 ps	445	______	______	555
		750 ps	693	______	______	808
		1 ns	0.940	______	______	1.060

Table 4–3: Test Record for HFS 9DG1 Card (Cont.)

Channel: ______	Page ______ of ______
Instrument Serial Number: ______	Certificate Number: ______
Temperature: ______	RH %: ______
Date of Calibration: ______	Technician: ______

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Pulse Width Limits 1% of width +50 –75ps						
Output Channel	Normal	5 ns	4.875	______	______	5.100
		10 ns	9.825	______	______	10.150
		50 ns	49.425	______	______	50.55
		100 ns	98.925	______	______	101.05
		500 ns	494.925	______	______	505.05
		1 µs	0.990	______	______	1.010
Not Output Channel	Normal	5 ns	4.875	______	______	5.100
		10 ns	9.825	______	______	10.150
		50 ns	49.425	______	______	50.55
		100 ns	98.925	______	______	101.05
		500 ns	494.925	______	______	505.05
		1 µs	0.990	______	______	1.010
Frequency Accuracy ± 1%						
Output Channel		50 kHz	49.50	______	______	50.50
		324 MHz	320.8	______	______	327.2
		326 MHz	322.7	______	______	329.3
		400 MHz	396.0	______	______	404.0
		433 MHz	428.7	______	______	437.3
		466 MHz	461.3	______	______	470.7
		500 MHz	495.0	______	______	505.0
		533 MHz	527.7	______	______	538.3
		566 MHz	560.3	______	______	571.7
		600 MHz	594.0	______	______	606.0
		630 MHz	623.7	______	______	636.3

Table 4–4: Test Record for HFS 9DG2 Card

Channel: ______	Page ______ of ______
Instrument Serial Number: ______	Certificate Number: ______
Temperature: ______	RH %: ______
Date of Calibration: ______	Technician: ______

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: ± 2% of level, ± 50 mV Low Level: ± 2% of High Level, ± 2% of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+5.5 V	+5.340	______	______	+5.660
	Normal	0.0 V	–0.270	______	______	+0.270
	Normal	–2.0 V	–2.090	______	______	–1.910
	Complement	–1.0 V	–1.070	______	______	–0.930
Rise Time / Fall Time ± 10% of setting ± 300 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	0.8 ns	0.420	______	______	1.180
	Complement, 1 V, Tf	0.8 ns	0.420	______	______	1.180
	Normal, 1 V, Tr	5 ns	4.200	______	______	5.800
	Complement, 1 V, Tf	5 ns	4.200	______	______	5.800
Edge Placement Pulse Delay Time 1% of (**Lead Delay** + **Chan Delay**) ±50 ps						
Output Channel	Normal	100 ps	49	______	______	151
		500 ps	445	______	______	555
		1 ns	0.940	______	______	1.060
		5 ns	4.900	______	______	5.100
		10 ns	9.850	______	______	10.150
		50 ns	49.45	______	______	50.55
		100 ns	98.95	______	______	101.05
Edge Placement Pulse Width Limits (1% + 50 ps, –450 ps) for widths < 20 ns (1% + 50 ps, –250 ps) for widths ≥ 20 ns						
Output Channel		5 ns	4.500	______	______	5.100
		10 ns	9.450	______	______	10.150
		50 ns	49.25	______	______	50.55
		100 ns	98.75	______	______	101.05
		500 ns	494.8	______	______	505.1
		1 µs	0.990	______	______	1.010
Frequency Accuracy ± 1%						
Output Channel		50 kHz	49.50	______	______	50.50
		162 MHz	160.4	______	______	163.6
		163 MHz	161.4	______	______	164.6
		200 MHz	198.0	______	______	202.0
		216.5 MHz	214.3	______	______	218.7
		233 MHz	230.7	______	______	235.3
		250 MHz	247.5	______	______	252.5
		266.5 MHz	263.8	______	______	269.2
		283 MHz	280.2	______	______	285.8
		300 MHz	297.0	______	______	303.0

Table 4–5: Test Record for HFS 9PG1 Card

Channel: ______			Page ______ of ______			
Instrument Serial Number: ______			Certificate Number: ______			
Temperature: ______			RH %: ______			
Date of Calibration: ______			Technician: ______			
Performance Test		**Nominal**	**Minimum**	**Incoming**	**Outgoing**	**Maximum**
Output High Level: ± 2% of level, ± 50 mV Low Level: ± 2% of High Level, ± 2% of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+2.6 V	+2.498	______	______	+2.702
	Normal	–0.4 V	–0.562	______	______	–0.238
	Normal	–2 V	–2.090	______	______	–1.910
	Complement	–1 V	–1.070	______	______	–0.930
Not Output Channel	Normal	+2.6 V	+2.498	______	______	+2.702
	Complement	–0.4 V	–0.562	______	______	–0.238
	Complement	–2 V	–2.090	______	______	–1.910
	Normal	–1 V	–1.070	______	______	–0.930
Rise Time / Fall Time ≤ 200 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	200 ps	N/A	______	______	200 ps
	Complement, 1 V, Tf	200 ps	N/A	______	______	200 ps
Not Output Channel	Normal, 1V, Tf	200 ps	N/A	______	______	200 ps
	Complement, 1 V, Tr	200 ps	N/A	______	______	200 ps
Edge Placement Pulse Delay Time 1% of (**Lead Delay** + **Chan Delay**) ±300 ps						
Output Channel	Normal	100 ps	–201	______	______	401
		500 ps	195	______	______	805
		1 ns	0.690	______	______	1.310
		5 ns	4.650	______	______	5.350
		10 ns	9.600	______	______	10.400
		50 ns	49.20	______	______	50.80
		100 ns	98.70	______	______	101.30
Not Output Channel	Normal	100 ps	–201	______	______	401
		500 ps	195	______	______	805
		1 ns	0.690	______	______	1.310
		5 ns	4.650	______	______	5.350
		10 ns	9.600	______	______	10.400
		50 ns	49.20	______	______	50.80
		100 ns	98.70	______	______	101.30
Edge Placement Pulse Width Variance 1% of width ± 300 ps						
Output Channel	Normal	500 ps	195	______	______	805
		750 ps	443	______	______	1060
		1 ns	0.690	______	______	1.310
Not Output Channel	Normal	500 ps	195	______	______	805
		750 ps	443	______	______	1058
		1 ns	0.690	______	______	1.310

Table 4–5: Test Record for HFS 9PG1 Card (Cont.)

Channel: ________	Page ________ of ________
Instrument Serial Number: ________	Certificate Number: ________
Temperature: ________	RH %: ________
Date of Calibration: ________	Technician: ________

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Pulse Width Limits 1% of width ± 300 ps						
Output Channel	Normal	5 ns	4.650	________	________	5.350
		10 ns	9.600	________	________	10.400
		50 ns	49.20	________	________	50.80
		100 ns	98.70	________	________	101.30
		500 ns	494.70	________	________	505.30
		1 µs	0.990	________	________	1.010
Not Output Channel	Normal	5 ns	4.650	________	________	5.350
		10 ns	9.600	________	________	10.400
		50 ns	49.20	________	________	50.80
		100 ns	98.70	________	________	101.30
		500 ns	494.70	________	________	505.30
		1 µs	0.990	________	________	1.010
Frequency Accuracy ± 1%						
Output Channel		50 kHz	49.50	________	________	50.50
		324 MHz	320.8	________	________	327.2
		326 MHz	322.7	________	________	329.3
		400 MHz	396.0	________	________	404.0
		433 MHz	428.7	________	________	437.3
		466 MHz	461.3	________	________	470.7
		500 MHz	495.0	________	________	505.0
		533 MHz	527.7	________	________	538.3
		566 MHz	560.3	________	________	571.7
		600 MHz	594.0	________	________	606.0
		630 MHz	623.7	________	________	636.3

Table 4–6: Test Record for HFS 9PG2 Card

Channel: ______	Page ______ of ______
Instrument Serial Number: ______	Certificate Number: ______
Temperature: ______	RH %: ______
Date of Calibration: ______	Technician: ______

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: ± 2% of level, ± 50 mV Low Level: ± 2% of High Level, ± 2% of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+5.5 V	+5.340	______	______	+5.660
	Normal	0 V	–0.270	______	______	+0.270
	Normal	–2 V	–2.090	______	______	–1.910
	Complement	–1 V	–1.070	______	______	–0.930
Not Output Channel	Normal	+5.5 V	+5.340	______	______	+5.660
	Complement	0 V	–0.270	______	______	+0.270
	Complement	–2 V	–2.090	______	______	–1.910
	Normal	–1 V	–1.070	______	______	–0.930
Rise Time / Fall Time ± 10% of setting ± 300 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	0.8 ns	0.420	______	______	1.180
	Complement, 1 V, Tf	0.8 ns	0.420	______	______	1.180
	Normal, 1 V, Tr	5 ns	4.200	______	______	5.800
	Complement, 1 V, Tf	5 ns	4.200	______	______	5.800
Not Output Channel	Normal, 1V, Tf	0.8 ns	0.420	______	______	1.180
	Complement, 1 V, Tr	0.8 ns	0.420	______	______	1.180
	Normal, 1 V, Tf	5 ns	4.200	______	______	5.800
	Complement, 1 V, Tr	5 ns	4.200	______	______	5.800
Edge Placement Pulse Delay Time 1% of (**Lead Delay** + **Chan Delay**) ±300 ps						
Output Channel	Normal	100 ps	–201	______	______	401
		500 ps	195	______	______	805
		1 ns	0.690	______	______	1.310
		5 ns	4.650	______	______	5.350
		10 ns	9.600	______	______	10.400
		50 ns	49.20	______	______	50.80
		100 ns	98.70	______	______	101.30
Not Output Channel	Normal	100 ps	–201	______	______	401
		500 ps	195	______	______	805
		1 ns	0.690	______	______	1.310
		5 ns	4.650	______	______	5.350
		10 ns	9.600	______	______	10.400
		50 ns	49.20	______	______	50.80
		100 ns	98.70	______	______	101.30

Table 4–6: Test Record for HFS 9PG2 Card (Cont.)

Channel: ____			Page ____ of ____			
Instrument Serial Number: ____			Certificate Number: ____			
Temperature: ____			RH %: ____			
Date of Calibration: ____			Technician: ____			
Performance Test		**Nominal**	**Minimum**	**Incoming**	**Outgoing**	**Maximum**
Edge Placement Pulse Width Limits (1% of width + 300 ps, –500 ps) for widths < 20 ns (1% of width, ± 300 ps) for widths > 20 ns						
Output Channel	Normal	5 ns	4.450	____	____	5.350
		10 ns	9.400	____	____	10.400
		50 ns	49.20	____	____	50.80
		100 ns	98.70	____	____	101.30
		500 ns	494.7	____	____	505.3
		1 µs	0.990	____	____	1.010
Not Output Channel	Normal	5 ns	4.450	____	____	5.350
		10 ns	9.400	____	____	10.400
		50 ns	49.20	____	____	50.80
		100 ns	98.70	____	____	101.30
		500 ns	494.7	____	____	505.3
		1 µs	0.990	____	____	1.010
Frequency Accuracy ± 1%						
Output Channel	Nominal = HFS Setting Output = Nominal/2	100 kHz	49.50	____	____	50.50
		324 MHz	160.4	____	____	163.6
		326 MHz	161.4	____	____	164.6
		400 MHz	198.0	____	____	202.0
		433 MHz	214.3	____	____	218.7
		466 MHz	230.7	____	____	235.3
		500 MHz	247.5	____	____	252.5
		533 MHz	263.8	____	____	269.2
		566 MHz	280.2	____	____	285.8
		600 MHz	297.0	____	____	303.0

Verification Sequence

The performance verification procedure consists of the following steps, performed in the following order:

1. Perform the HFS 9000 internal self test that follows this list of steps. If the self test indicates problems, refer to the *Maintenance* section in the Service Manual to repair the instrument.
2. Perform the internal calibration on page 4–12 if the HFS 9000 has not been recalibrated within the last six months, or if the HFS 9000 has been reconfigured with different cards or has been adjusted or repaired.
3. Follow the procedures in the Check Procedures section beginning on page 4–13 to verify that the HFS 9000 performs to every specification.

Self Test

The HFS 9000 is equipped with self-test diagnostic routines that execute automatically when you switch the power on. You may also manually select the diagnostic routines.

Use the following procedure to manually select the diagnostic routines:

1. Press **MAIN MENU** and select **Cal/Deskew Menu**.
2. Select **Self Test**.

The HFS 9000 display indicates the circuits under test as it proceeds through the diagnostics. The HFS 9000 returns to normal operating mode after successfully completing the diagnostics.

If the HFS 9000 detects a failure, it suspends normal operation and displays an error code (see the *Maintenance* section in the Service Manual for further information). The display presents two choices:

- Press any button other than the **SELECT** button to show a terse description of the failure. This additional information may assist you in isolating a failure to a module, or to determine if users can continue to operate the HFS 9000. The next diagnostic test will not begin until you press the **SELECT** button.
- Press the **SELECT** button to continue with the next diagnostic test.

A self-test failure does not necessarily indicate that the HFS 9000 is inoperable. However, it does indicate that the instrument is out of specification and that it might not be fully operational.

Calibration

The calibration procedure adjusts the instrument to its internal voltage and timing references and saves the settings in non-volatile memory.

Calibrate the HFS 9000 at least every six months. The instrument does not need more frequent calibration unless it is reconfigured or used in an ambient temperature that differs by more than 5° C from the temperature it was last calibrated in.

***NOTE**. Run the calibration procedure only when the HFS 9000 has been powered on for 20 minutes in the temperature environment you expect it to be used in.*

To calibrate the HFS 9000, select the **Calibrate** item in the Cal/Deskew menu.

After you select the Calibrate item, verify this choice in the subsequent dialog box. After verification, the HFS 9000 starts the Timebase calibration and prompts you to attach an SMA cable from the front panel SKEW CAL IN connector to the TRIGGER OUT connector. The HFS 9000 then prompts you to connect each channel OUTPUT connector in turn. The HFS 9000 performs the calibration automatically during the time that each channel is connected. The time for the calibration procedure varies by configuration.

A 20 inch, 50 Ω coaxial SMA cable (Tektronix part number 174-1427-00) is supplied with the HFS 9000 as a standard accessory. This cable is suitable for use during calibration.

Check Procedures

Once you have run the self-test procedure, and, if necessary, calibrated the HFS 9000, these check procedures will verify that the instrument performs as specified.

Instrument Setup

Select **MAIN MENU** and reset the HFS 9000 using the **Reset** item in the Save/Recall menu. After this reset, the parameters listed below are properly set for all tests and need not be modified again. However, each check specifies a reset as a first step to ensure the following settings:

- Cal/Deskew menu, **Pretrigger** item: 70 ns
- Cal/Deskew menu, **Channel Delay** item: 0 s (all channels)
- Time Base menu, **Mode** item: Auto
- Levels menu, **Limit** item: Off
- Pulse menu, **Signal Type** item: Pulse

***NOTE**. Allow the HFS 9000 to warm up for a minimum of 20 minutes. The instrument must warm up in an ambient temperature within 5° C of the ambient temperature when last calibrated.*

After you have set up the first channel for a particular check, use the **Copy Channel** and **Paste Channel** menu items to transfer the setup to the other channels.

Output Level Checks (HFS 9DG1 Card Only)

These tests check the output level in volts DC of each data generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to “the channel” is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1)
	One BNC female to dual banana connector (item 2)
	One precision coaxial cable (item 3)
	One feedthrough termination (item 4)
	One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000.
2. Set the Digital Voltmeter to measure DC volts on Auto Range.

3. Construct the termination assembly by connecting the following items in the order listed:

   a. one BNC female to dual banana connector (item 2)

   b. one precision coaxial cable (item 3)

   c. one feedthrough termination (item 4)

   d. one BNC female to SMA male adapter (item 10)

   e. one threaded SMA female to SMA male slip-on connector (item 11).

4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.

5. Set the HFS 9000 according to Table 4–7.

Table 4–7: HFS 9DG1 Output Level Checks, First Settings

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **Output**	On
Pulse menu, **~Output**	Off
Pulse menu, **Pulse Rate**	Off
Pulse menu, **Polarity**	Complement
Pulse menu, **High Level**	5.0 V
Pulse menu, **Low Level**	2.0 V

The output voltage reading on the DVM should be between 4.850 V and 5.150 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

   The output voltage reading on the DVM should be between 1.790 V and 2.210 V.

7. Set the HFS 9000 according to Table 4–8.

Table 4–8: HFS 9DG1 Output Level Checks, Second Settings

Control	Setting
Pulse menu, **High Level**	–1.5 V
Pulse menu, **Low Level**	–2.5 V

The output voltage reading on the DVM should be between –2.680 V and –2.320 V.

8. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –1.580 V and –1.420 V.

9. Move the feedthrough termination assembly to the channel complemented $\overline{\text{OUTPUT}}$. The DVM is now set to monitor the complement output.

10. Set the HFS 9000 according to Table 4–9.

Table 4–9: HFS 9DG1 Output Level Checks, Third Settings

Control	Setting
Pulse menu, **Output**	Off
Pulse menu, **~Output**	On
Pulse menu, **Polarity**	Normal
Pulse menu, **High Level**	5.0 V
Pulse menu, **Low Level**	2.0 V

The output voltage reading on the DVM should be between 4.850 V and 5.150 V.

11. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between 1.790 V and 2.210 V.

12. Set the HFS 9000 according to Table 4–10.

Table 4–10: HFS 9DG1 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, **High Level**	–1.5 V
Pulse menu, **Low Level**	–2.5 V

The output voltage reading on the DVM should be between –2.680 V and –2.320 V.

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –1.580 V and –1.420 V.

14. Repeat steps 1 through 13 for each of the HFS 9DG1 channels in the system.

15. Disconnect test setup.

Output Level Checks (HFS 9DG2 and HFS 9PG2 Cards Only)

These tests check the output level in volts DC of each pulse or data generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to "the channel" is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1) One BNC female to dual banana connector (item 2) One precision coaxial cable (item 3) One feedthrough termination (item 4) One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000.

2. Set the Digital Voltmeter to measure DC volts on Auto Range.

3. Construct the termination assembly by connecting the following items in the order listed:

- **a.** one BNC female to dual banana connector (item 2)
- **b.** one precision coaxial cable (item 3)
- **c.** one feedthrough termination (item 4)
- **d.** one BNC female to SMA male adapter (item 10)
- **e.** one threaded SMA female to SMA male slip-on connector (item 11).

4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.

5. Set the HFS 9000 according to Table 4–11.

Table 4–11: HFS 9DG2 and HFS 9PG2 Output Level Checks, First Settings

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **Output**	On
Pulse menu, **~Output**	Off
Pulse menu, **Pulse Rate**	Off
Pulse menu, **Polarity**	Complement
Pulse menu, **High Level**	5.5 V
Pulse menu, **Low Level**	0 V

The output voltage reading on the DVM should be between 5.340 V and 5.660 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

   The output voltage reading on the DVM should be between –0.270 V and +0.270 V.

7. Set the HFS 9000 according to Table 4–12.

Table 4–12: HFS 9DG2 and HFS 9PG2 Output Level Checks, Second Settings

Control	Setting
Pulse menu, **High Level**	–1.0 V
Pulse menu, **Low Level**	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

8. Change the Pulse menu **Polarity** item setting to **Complement**.

   The output voltage reading on the DVM should be between –1.070 V and –0.930 V.

9. Move the feedthrough termination assembly to the channel complemented $\overline{\text{OUTPUT}}$ if available (HFS 9PG2). The DVM is now set to monitor the complement output.

10. Set the HFS 9000 according to Table 4–13.

Table 4–13: HFS 9PG2 Output Level Checks, Third Settings

Control	Setting
Pulse menu, **Output**	Off
Pulse menu, **~Output**	On
Pulse menu, **Polarity**	Normal
Pulse menu, **High Level**	5.5 V
Pulse menu, **Low Level**	0 V

The output voltage reading on the DVM should be between 5.340 V and 5.660 V.

11. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –0.270 V and +0.270 V.

12. Set the HFS 9000 according to Table 4–14.

Table 4–14: HFS 9PG2 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, **High Level**	–1.0 V
Pulse menu, **Low Level**	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

14. Repeat steps 1 through 13 for each of the HFS 9PG2 and HFS 9DG2 channels in the system.

15. Disconnect test setup.

Output Level Checks (HFS 9PG1 Card Only)

These tests check the output level in volts DC of each pulse generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to "the channel" is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1) One BNC female to dual banana connector (item 2) One precision coaxial cable (item 3) One feedthrough termination (item 4) One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000.
2. Set the Digital Voltmeter to measure DC volts on Auto Range.
3. Construct the termination assembly by connecting the following items in the order listed:
   a. one BNC female to dual banana connector (item 2)
   b. one precision coaxial cable (item 3)
   c. one feedthrough termination (item 4)
   d. one BNC female to SMA male adapter (item 10)
   e. one threaded SMA female to SMA male slip-on connector (item 11).
4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.
5. Set the HFS 9000 according to Table 4–15.

Table 4–15: HFS 9PG1 Output Level Checks, First Settings

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **Output**	On
Pulse menu, **~Output**	Off
Pulse menu, **Pulse Rate**	Off
Pulse menu, **Polarity**	Complement
Pulse menu, **High Level**	2.6 V
Pulse menu, **Low Level**	–0.4 V

The output voltage reading on the DVM should be between 2.498 V and 2.702 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

   The output voltage reading on the DVM should be between –0.562 V and –0.238 V.

7. Set the HFS 9000 according to Table 4–16.

Table 4–16: HFS 9PG1 Output Level Checks, Second Settings

Control	Setting
Pulse menu, **High Level**	–1.0 V
Pulse menu, **Low Level**	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

8. Change the Pulse menu **Polarity** item setting to **Complement**.

   The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

9. Move the feedthrough termination assembly to the channel complemented $\overline{\text{OUTPUT}}$. The DVM is now set to monitor the complement output.

10. Set the HFS 9000 according to Table 4–17.

Table 4–17: HFS 9PG1 Output Level Checks, Third Settings

Control	Setting
Pulse menu, **Output**	Off
Pulse menu, **~Output**	On
Pulse menu, **Polarity**	Normal
Pulse menu, **High Level**	2.6 V
Pulse menu, **Low Level**	–0.4 V

The output voltage reading on the DVM should be between 2.498 V and 2.702 V.

11. Change the Pulse menu **Polarity** item setting to **Complement**.

    The output voltage reading on the DVM should be between –0.562 V and –0.238 V.

12. Set the HFS 9000 according to Table 4–18.

Table 4–18: HFS 9PG1 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, **High Level**	–1.0 V
Pulse menu, **Low Level**	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

14. Repeat steps 1 through 13 for each of the HFS 9PG1 channels in the system.

15. Disconnect test setup.

Trigger Output Level

This check verifies the level of the HFS 9000 trigger output.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8)

1. Connect an SMA cable from the HFS 9000 **TRIGGER OUTPUT** to the Channel 1 input of the DSO sampling head.

2. Connect an SMA cable from the DSO trigger input to the HFS 9000 Channel 1 output.

3. Reset the HFS 9000.

4. Initialize the DSO and select the Channel 1 sampling head input.

5. Press **AUTOSET** and set the HFS 9000 and DSO according to Table 4–19.

Table 4–19: Settings for Trigger Output Check

Control	Setting
HFS 9000:	
Pulse menu, **Period**	Press **SELECT** to change the **Period** item to a **Frequency** item
Pulse menu, **Frequency**	100 MHz
Pulse menu, **Output**	On
DSO:	
Main Size	2 ns
Vertical Size	200 mV
Vertical Offset	0
Main Position	Minimum
Measure	Min, Max, Amplitude

6. Measure maximum value is less than or equal to –0.5 V, the minimum value is greater than or equal to –1.5 V and the amplitude is greater than or equal to 300 $mV_{p\text{-}p}$.

Rise Time and Fall Time Checks (HFS 9PG1 and HFS 9DG1 Cards Only)

These checks verify the rise time and fall times of HFS 9PG1 pulse card and HFS 9DG1 data time generator channels. You will check each HFS 9000 high speed channel in turn. A reference to "the channel" is a reference to the particular channel under test.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6)
	Two SMA coaxial cables (item 8)
	One SMA 5X attenuator (item 7)
	One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000, then make the settings according to Table 4–20.

Table 4–20: Settings for Rise Time and Fall Time Checks

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **High Level**	Press **SELECT** to change the **High Level** item to an **Amplitude** item, and the **Low Level** item to an **Offset** item
Pulse menu, **Amplitude**	1.0 V
Pulse menu, **Offset**	0 V
Pulse menu, **Polarity**	Normal
Pulse menu, **Period**	Press **SELECT** to change the **Period** item to a **Frequency** item
Pulse menu, **Frequency**	100 kHz
Pulse menu, **Pulse Rate**	Normal
Pulse menu, **Output**	On
Pulse menu, **~Output**	Off

2. Initialize the DSO.
3. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO. Set the DSO to trigger on that signal. Turn on averaging on the DSO.

CAUTION. *To avoid accidentally damaging the sampling head of the DSO, place a 5X SMA attenuator on the sampling head input. Voltages in excess of 3 volts may damage the input circuit.*

4. After placing a 5X SMA attenuator on the sampling head input, connect an SMA cable from the 5X SMA attenuator to the HFS 9000 normal **OUTPUT** connector of the channel under test. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.
5. Set the DSO to display the signal with 50 mV/div (4 divisions) vertically at zero offset. Set the DSO time base to 1 μs/div horizontally. Set the DSO **MAIN POSITION** to minimum.

6. Display the DSO measurement menu and turn on **RISE** and **FALL** measurements. Touch the **RISE** selector at the bottom of the DSO screen to display the **RISE** measurement parameters. Set these parameters according to Table 4–21.

Table 4–21: DSO Settings for Rise/Fall Time Checks

DSO Control	Setting
Left Limit	0%
Right Limit	100%
Proximal	20%
Distal	80%
Tracking	On
Level Mode	Relative

7. Once the DSO captures high and low levels, turn off tracking.
8. Set the DSO sweep speed to 500 ps/div and position the first rising edge at center screen. The measured rise time should be less than 200 ps for HFS 9PG1 cards, and less than 250 ps for a HFS 9DG1 cards. (Use waveform averaging to stabilize the measurement.)
9. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time should be less than 200 ps for HFS 9PG1 cards, and less than 250 ps for HFS 9DG1 cards.
10. Repeat steps 1 through 9 for each of the HFS 9PG1 or HFS 9DG1 card channels in the system. (For Not Output channels, set **Output** off and **~Output** on.)
11. Disconnect test setup.

Rise Time and Fall Time Checks (HFS 9PG2 and HFS 9DG2 Cards Only)

These checks verify the rise time and fall times of HFS 9PG2 pulse card and HFS 9DG2 data time generator channels. You will check each HFS 9000 high speed channel in turn. A reference to "the channel" is a reference to the particular channel under test.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8) One SMA 5X attenuator (item 7) One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000, then make the settings listed in Table 4–22.

Table 4–22: Settings for Rise Time and Fall Time Checks

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **High Level**	Press **SELECT** to change the **High Level** item to an **Amplitude** item, and the **Low Level** item to a **Offset** item
Pulse menu, **Amplitude**	1.0 V
Pulse menu, **Offset**	0 V
Pulse menu, **Polarity**	Normal
Pulse menu, **Transition**	800 ps
Pulse menu, **Period**	Press **SELECT** to change the **Period** item to a **Frequency** item
Pulse menu, **Frequency**	100 kHz
Pulse menu, **Pulse Rate**	Normal
Pulse menu, **Output**	On
Pulse menu, **~Output**	Off

2. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO. Set the DSO to trigger on that signal.

CAUTION. *To avoid accidentally damaging the sampling head of the DSO, place a 5X SMA attenuator on the sampling head input. Voltages in excess of 3 volts may damage the input circuit.*

3. After placing a 5X SMA attenuator on the sampling head input, connect an SMA cable from the 5X SMA attenuator to the HFS 9000 normal **OUTPUT** connector of the channel under test. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.

4. Set the DSO to display the signal with 50 mV/div (4 divisions) vertically at zero offset. Set the DSO time base to 1 μs/div horizontally. Set the DSO **MAIN POSITION** to minimum.

5. Display the DSO measurement menu and turn on **RISE** and **FALL** measurements. Touch the **RISE** selector at the bottom of the DSO screen to display the **RISE** measurement parameters. Set these parameters according to Table 4–23.

Table 4–23: DSO Settings for Rise/Fall Time Checks

DSO Control	Setting
Left Limit	0%
Right Limit	100%
Proximal	20%
Distal	80%
Tracking	On
Level Mode	Relative

6. Once the DSO captures high and low levels, turn off tracking.

7. Set the DSO sweep speed to 500 ps/div and position the first rising edge at center screen. The measured rise time should be between 420 ps and 1.18 ns (HFS 9PG2 & HFS 9DG2 cards). (Use waveform averaging to stabilize the measurement.)

8. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time should be between 420 ps and 1.18 ns (HFS 9PG2 & HFS 9DG2 cards).

9. Change the Pulse menu **Polarity** item setting to Normal. Set the Pulse menu **Transition** item to 5 ns.

10. Set the DSO time base to 5 ns/div. Use the RISE measurement to verify that the rise time is between 4.2 ns and 5.8 ns (HFS 9PG2 & HFS 9DG2 cards).

11. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time on the DSO should be between 4.2 ns and 5.8 ns (HFS 9PG2 & HFS 9DG2 cards).

12. Repeat steps 1 through 11 for each of the HFS 9PG2 or HFS 9DG2 card channels in the system. (For Not Output channels, set **Output** off and **~Output** on.)

13. Disconnect test setup.

Edge Placement Checks

These checks verify the accuracy of the pulse delays and pulse widths. You will check each HFS 9000 channel in turn. A reference to "the channel" is a reference to the particular channel being checked in this repetition.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8) One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000, then make the settings according to Table 4–24.

Table 4–24: Settings for Edge Placement Checks

Control	Setting
Pulse menu, **Channel**	The channel under test
Pulse menu, **High Level**	Press **SELECT** to change the **High Level** item to an **Amplitude** item, and the **Low Level** item to an **Offset** item
Pulse menu, **Amplitude**	1.0 V
Pulse menu, **Offset**	0 V
Pulse menu, **Period**	Press **SELECT** to change the **Period** item to a **Frequency** item
Pulse menu, **Frequency**	100 kHz
Pulse menu, **Output**	On

2. If the channel is a Variable Rate (HFS 9PG2 or HFS 9DG2) channel, set transition to the lowest (fastest) rise time possible. (A quick way to do this is to enter "0" on the numeric keypad.)

3. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO.

4. Connect an SMA cable from the normal **OUTPUT** connector of the HFS 9000 channel under test to the sampling head input of the DSO. To save

time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.

5. Initialize the DSO, then set the DSO to display a triggered signal with 200 mV/div (5 divisions) vertically at zero offset. Set the DSO time base to 1 μs/div horizontally. Set the DSO **MAIN POSITION** to minimum.

6. Display the DSO measurement menu and turn on **WIDTH** and **CROSS** measurements. On the DSO, touch the **WIDTH** selector at the bottom of the DSO screen to display the width measurement parameters. Set the DSO width **LEVEL MODE** parameter to **RELATIVE**. Turn the DSO tracking on.

7. On the DSO, turn tracking off when the high and low levels have been acquired.

8. Set the DSO sweep speed to 500 ps/div. Position the rising edge of the displayed waveform at the center of the DSO screen. On the DSO, save the cross measurement as the reference (in the Compare & References pop-up menu).

9. On the DSO, turn **COMPARE** on.

10. Refer to Table 4–25 or 4–26, as appropriate, and adjust for each of the specified Pulse menu **Lead Delay** settings listed in the left column. For each **Lead Delay** value, verify that the DSO CROSS measurement falls within the limits specified in the middle and right columns. You may need to adjust the DSO horizontal position to keep the rising edge on the screen.

Table 4–25: Lead Delay Limits for HFS 9PG1 and HFS 9PG2

HFS 9000 Pulse Menu Lead Delay Setting	DSO CROSS Measurement Minimum	DSO CROSS Measurement Maximum
100 ps	–201 ps	401 ps
500 ps	195 ps	805 ps
1 ns	690 ps	1.31 ns
5 ns	4.65 ns	5.35 ns
10 ns	9.60 ns	10.4 ns
50 ns	49.2 ns	50.8 ns
100 ns	98.7 ns	101.3 ns

Table 4–26: Lead Delay Limits for HFS 9DG1 and HFS 9DG2

HFS 9000 Pulse Menu Lead Delay Setting	DSO CROSS Measurement Minimum	DSO CROSS Measurement Maximum
100 ps	49 ps	151 ps
500 ps	445 ps	555 ps
1 ns	940 ps	1.060 ns
5 ns	4.9 ns	5.1 ns
10 ns	9.85 ns	10.15 ns
50 ns	49.45 ns	50.55 ns
100 ns	98.95 ns	101.05 ns

11. Set the DSO horizontal position to minimum. Turn the DSO COMPARE off.

12. On the HFS 9000, use the **SELECT** button to change the Pulse menu **Duty Cycle** item to a **Width** item. Set the **Lead Delay** item to zero.

13. Skip this step if the channel is a Variable Rate (HFS 9PG2 or HFS 9DG2) channel. Refer to Table 4–27 or Table 4–28. Adjust the DSO horizontal position to display the first rising edge at screen. While observing the width measurement readout on the DSO, adjust the HFS 9000 **Pulse Width** item with the knob in **Fine** mode until each reading in the left column is achieved on the DSO. Then, observe the **Width** item setting on the HFS 9000 that achieved this result. Verify that the HFS 9000 value is within the limits specified in the middle and right columns. You may need to adjust the DSO horizontal position to keep the pulse on the screen.

Table 4–27: Width Variance Limits for HFS 9PG1

DSO WIDTH Measurement Readout	HFS 9000 Width Setting Minimum	HFS 9000 Width Setting Maximum
500 ps	195 ps	805 ps
750 ps	443 ps	1.06 ns
1 ns	690 ps	1.31 ns

Table 4–28: Width Variance Limits for HFS 9DG1

DSO WIDTH Measurement Readout	HFS 9000 Width Setting Minimum	HFS 9000 Width Setting Maximum
650 ps	594 ps	732 ps
750 ps	693 ps	833 ps
1 ns	940 ps	1.085 ns

14. Refer to Tables 4–29, 4–30 and 4–31, as appropriate, and set each of the specified Pulse menu **Width** settings listed in the left column. For each **Width** setting, verify that the DSO WIDTH measurement falls within the limits specified in the middle and right columns. Adjust the horizontal time/division as necessary to keep a full pulse displayed on screen.

Table 4–29: Width Limits for HFS 9PG1 and HFS 9PG2

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum		DSO WIDTH Measurement Maximum
	HFS 9PG1	HFS 9PG2	
5 ns	4.65 ns	4.45 ns	5.35 ns
10 ns	9.60 ns	9.40 ns	10.4 ns
50 ns	49.2 ns	49.2 ns	50.8 ns
100 ns	98.7 ns	98.7 ns	101.3 ns
500 ns	494.7 ns	494.7 ns	505.3 ns
1 µs	990 ns	990 ns	1.01 µs

Table 4–30: Width Limits for HFS 9DG1

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum	DSO WIDTH Measurement Maximum
5 ns	4.875 ns	5.1 ns
10 ns	9.825 ns	10.15 ns
50 ns	49.45 ns	50.55 ns
100 ns	98.95 ns	101.05 ns
500 ns	494.95 ns	505.05 ns
1 µs	990 ns	1.01 µs

Table 4–31: Width Limits for HFS 9DG2 1

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum	DSO WIDTH Measurement Maximum
5 ns	4.500 ns	5.1 ns
10 ns	9.450 ns	10.15 ns
50 ns	49.25 ns	50.55 ns
100 ns	98.75 ns	101.05 ns
500 ns	494.8 ns	505.1 ns
1 μs	990 ns	1.01 μs

15. Repeat steps 1 through 14 for each of the channels in the system. (For Not Output channels, set **Output** off and **~Output** on).

16. Disconnect test setup.

Frequency Accuracy Check

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) One SMA coaxial cable (item 8) One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000, then use the SELECT button to change the Pulse menu **Period** item to a **Frequency** item.

2. Connect an SMA cable from the HFS 9000 TRIGGER OUT connector to the DIRECT connector located in the TRIGGER INPUTS section of the DSO. Set the DSO to trigger on that signal.

3. Connect an SMA cable from the normal OUTPUT connector of any High Speed HFS 9000 channel to the sampling head input of the DSO. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.

***NOTE**. If you have any HFS 9PG2 channels, set the Pulse menu **Pulse Rate** item to Half for those channels. If you have Variable Rate or HFS 9DG2 channels, use one of them for this test.*

4. Turn on the output of the HFS 9000 channel you are using.

5. Set the DSO to display the signal with 200 mV/div vertically and a vertical offset of –1.3 V. Set the DSO time base to 500 ps/div horizontally. Set the DSO MAIN POSITION to minimum.

6. Display the DSO measurement menu and turn on the FREQUENCY measurement. On the DSO, turn TRACKING on and turn on AVERAGING with AVGN set to 32.

7. Refer to Tables 4–32, 4–33, or 4–34 as appropriate, and adjust for each of the specified Pulse menu **Frequency** settings listed in the left column. For each **Frequency** value, verify that the DSO FREQUENCY measurement falls within the limits specified in the middle and right columns. Adjust the horizontal size and position to make the display of a single cycle fill the DSO screen.

Table 4–32: Frequency Limits (HFS 9PG1 & HFS 9DG1)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY Minimum	DSO FREQUENCY Maximum
50 kHz	49.5 kHz	50.5 kHz
324 MHz	320.8 MHz	327.2 MHz
326 MHz	322.7 MHz	329.3 MHz
400 MHz	396.0 MHz	404.0 MHz
433 MHz	428.7 MHz	437.3 MHz
466 MHz	461.3 MHz	470.7 MHz
500 MHz	495.0 MHz	505.0 MHz
533 MHz	527.7 MHz	538.3 MHz
566 MHz	560.3 MHz	571.7 MHz
600 MHz	594.0 MHz	606.0 MHz
630 MHz	623.7 MHz	636.3 MHz

Table 4–33: Frequency Limits (HFS 9PG2)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY (÷ 2) Minimum	DSO FREQUENCY (÷ 2) Maximum
100 kHz	49.5 kHz	50.5 kHz
324 MHz	160.4 MHz	163.6 MHz
326 MHz	161.4 MHz	164.6 MHz
400 MHz	198 MHz	202 MHz
433 MHz	214.3 MHz	218.7 MHz

Table 4–33: Frequency Limits (HFS 9PG2) (Cont.)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY (÷ 2) Minimum	DSO FREQUENCY (÷ 2) Maximum
466 MHz	230.7 MHz	235.3 MHz
500 MHz	247.5 MHz	252.5 MHz
533 MHz	263.8 MHz	269.2 MHz
566 MHz	280.2 MHz	285.8 MHz
600 MHz	297.0 MHz	303.0 MHz

Table 4–34: Frequency Limits (HFS 9DG2)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY Minimum	DSO FREQUENCY Maximum
50 kHz	49.5 kHz	50.5 kHz
162 MHz	160.4 MHz	163.6 MHz
163 MHz	161.4 MHz	164.6 MHz
200 MHz	198.0 MHz	202.0 MHz
216.5 MHz	214.3 MHz	218.7 MHz
233 MHz	230.7 MHz	235.3 MHz
250 MHz	247.5 MHz	252.5 MHz
266.5 MHz	263.8 MHz	269.2 MHz
283 MHz	280.2 MHz	285.8 MHz
300 MHz	297.0 MHz	303.0 MHz

Phase Lock Check

Equipment Required	Generator, Leveled Sine Wave (item 9) BNC female to SMA male adapter (item 10).

This check verifies that the phase lock system is capable of detecting, accurately measuring, and holding an input signal.

***NOTE**. If the HFS 9003 cannot determine the phase lock frequency, an error message is displayed. This will happen if the phase lock signal is not stable and continuous, or if the phase lock signal is outside the allowed frequency range, or if the HFS 9003 needs calibrating.*

1. Reset the HFS 9000.
2. Set the signal generator for an amplitude of 0.8 V_{p-p} and a frequency of 250 MHz. Connect the signal to the HFS 9000 **PHASE LOCK IN** connector. If your generator does not have better than 1% frequency accuracy, use the FREQUENCY measurement capability of the DSO to set the generator frequency to within 1%.
3. Set the Time Base menu **PhaseLockIn** item to On.
4. Check that the input frequency is correctly displayed on the HFS 9000 screen immediately above the menu area.
5. Wait at least five seconds and make sure that the HFS 9000 retains phase lock. (If phase lock is lost, you will see an error message.)
6. Set the Time Base menu **PhaseLockIn** item to Off.
7. Repeat steps 3 through 6 with the signal generator set to 594 MHz. If your generator does not have better than 1% frequency accuracy, use the FREQUENCY measurement capability of the DSO to set the generator frequency to within 1%.
8. You may optionally check other frequencies as well. Low frequency checks will require a different generator (such as a square wave generator) which meets to 20% to 80% risetime requirement of 10 ns or less for the **PHASE LOCK IN** input.
9. Disconnect test setup.

Adjustment Procedures

The only adjustments that can be made to the HFS 9003 are to the power supply outputs. No other circuitry in the instrument requires or has adjustments.

The power supply voltages are measured and adjusted under no-load conditions. Adjustments should be made only if the output voltages are out of tolerance. If a supply cannot be adjusted to within tolerance, the module must be replaced.

Required Test Equipment

You will need a digital voltmeter (DVM) with 0.3% accuracy ranging from 2 VDC to 24 VDC.

Disassembly for Adjustment

See the removal procedure for the power supplies on page 6–5.

⚠ ***WARNING.*** *To avoid electric shock, disconnect the power source when removing or replacing the covers. Hazardous voltages are exposed when the covers are removed, even when the power switch is in the* ***STANDBY*** *position. Use extreme caution when the instrument is connected to a power source while the covers are removed.*

Adjustment

Only make adjustments to supply voltages that measure outside the range in Table 5–1 under no-load conditions. Voltage measurements can be read from the spade connectors located on the back of the backplane or from the spade connectors on the supplies themselves. Refer to Figures 5–1 and 5–2 for the voltage assignments.

The voltage levels are adjusted with the potentiometers located near the edge of the power supply modules. On the supply closest to the rear, the three potentiometers from top to bottom set the +5 V, +12 V, and –12 V levels respectively. For the supply closest to the front of the instrument, the potentiometers from top to bottom set +24 V, –2 V, and –5.2 V respectively.

Table 5–1: Power Supply Tolerances

Nominal Voltage	Supply Module	Acceptable Range
+5 V	Rear	4.875 V to 5.25 V
+12 V	Rear	11.54 V to 12.60 V
–12 V	Rear	–11.64 V to –12.60 V
–2 V	Front	–1.9 V to –2.1 V
–5.2 V	Front	–5.044 V to –5.46 V
+24 V	Front	23.28 V to 25.20 V

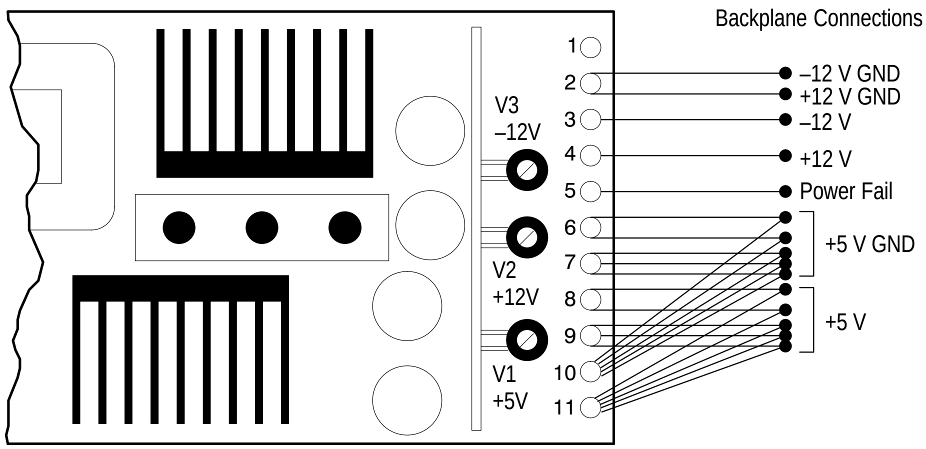


Figure 5–1: Rear Power Supply Voltage and Adjustment Locations

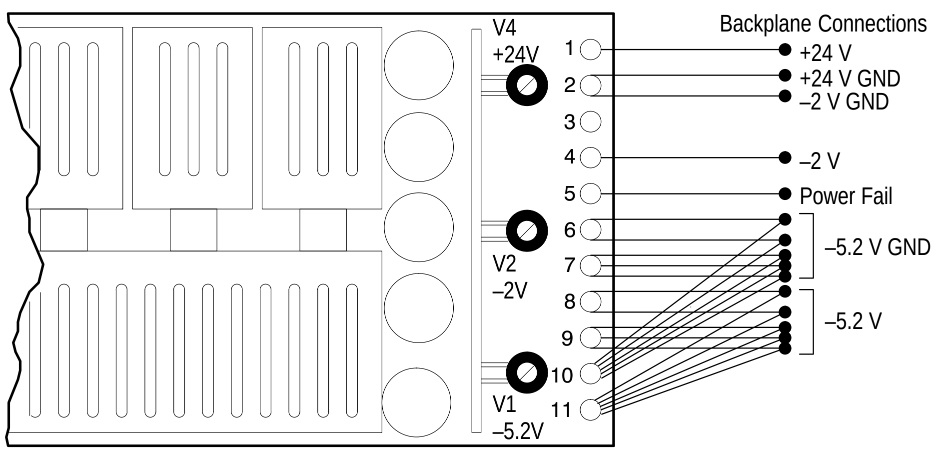


Figure 5–2: Front Power Supply Voltage and Adjustment Locations

Preventive Maintenance

Accumulations of dirt impair the efficiency of the cooling fans and reduce heat transfer from components. Dirt may also cause faulty operation of the fan speed control temperature sensor. Periodically vacuum dirt and dust from the inside of the mainframe, paying particular attention to the fans. Heavy accumulations of dirt should be removed with a soft brush. Change the fan filters when necessary.

CAUTION. *To avoid damage to electrical contacts, do not use water or alcohol to clean the backplane card connectors.*

The HFS 9003 is designed to require no adjustment under normal conditions.

Removal and Replacement

The removal and replacement procedures describe the disassembly of the HFS 9003 to service the instrument. Observe all cautions and warnings. Refer to the *Diagrams* section of this manual for a block diagram of the HFS 9003.

Front Panel Module

The Front Panel module, which contains the display and keypad, is a single Field Replaceable Unit. Turn off instrument power when removing or installing the front panel module.

Removal

1. Remove the two screws holding on the front panel, one under each corner on both sides.
2. Swing the bottom of the front panel module away from the instrument, then lift the module off the two hooks it hangs from.
3. Disconnect the ribbon cable connecting the front panel module to the CPU card. Mark it for proper reconnection.

Replacement

1. Connect the ribbon cable between the front panel module and the CPU card.
2. Hang the top of the front panel module from the hooks at the top corners of the mainframe, then swing the bottom of the front panel flush. Make sure all clock distribution cables are positioned in the channel in the back of the front panel module.
3. Install the two screws holding the bottom of the front panel module in place; one is located underneath the front panel module on each side.

Cards

Pulse or data generator cards are behind the small panels in the open area of the front panel. Turn off instrument power when removing or installing cards.

Removal

1. Remove the front panel module as described on page 6–3.
2. If the card you are removing is the time base card or any pulse or data generator card, remove the clock distribution cable (see Figure 6–1).

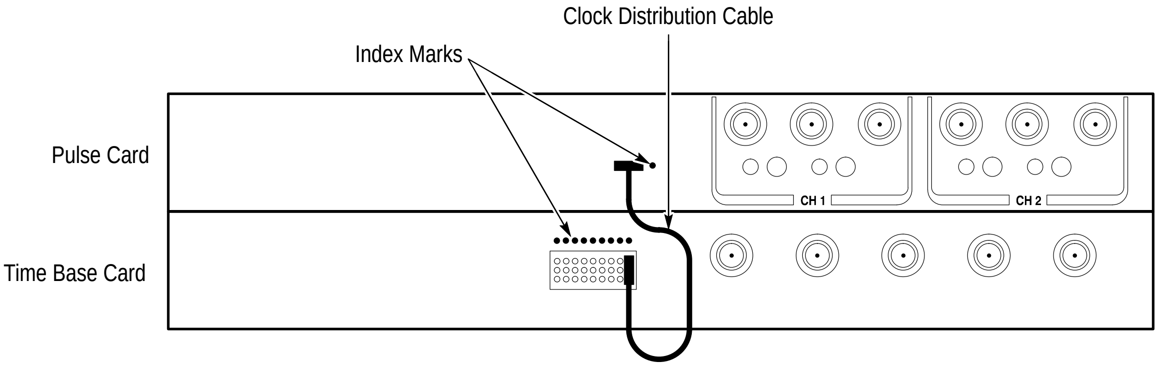


Figure 6–1: Clock Distribution Cable Location

3. Each card is fastened with two screws, one on either end of the card front panel. Remove these screws, and pull the card straight forward.

Replacement

1. Push the card into the appropriate slot through in the mainframe. Refer to the Block Diagram (see Figure 9–1 on page 9–2) to identify the proper card position in the rack. Secure the card with two screws, one on either end of the card front panel.

2. If the card is a pulse or data generator card or the time base card, reinstall the clock distribution cables. Align the index mark on the cable connectors with the index marks on the card. When all cards are installed, a clock distribution cable must connect the time base card to each pulse or data generator card (see Figure 6–1). The time base card has several connectors for clock distribution cables; it does not matter which of these connectors is used for each pulse or data generator card.

Mainframe Covers

For most mainframe service operations, only the top cover needs to be removed from the mainframe.

WARNING. *To avoid electric shock, disconnect the power source when removing or replacing the covers. Hazardous voltages are exposed when the covers are removed, even when the power switch is in the standby position. Use extreme caution when the product is connected to the power source while the covers are removed.*

Removal The top and bottom covers are fastened with fourteen screws each. Four screws are located on each side along the edge of the cover, and three screws are located along the front and rear edges. After removing the screws, the covers may be lifted off.

Replacement Place the cover on the frame, making sure the ventilation holes are oriented over the cooling fans. Install and tighten the fourteen screws.

Power Supply Assembly

WARNING. *To avoid electric shock, allow at least five minutes discharge time after disconnecting power before attempting any service to the power supply assembly. Several capacitors in the power supply assembly retain a substantial charge (up to 660 Volts) after power is disconnected.*

Removal

1. Remove the top cover of the mainframe as described on page 6–4.
2. Remove the ten screws from the top cover of the power supply assembly and remove the top cover.
3. Remove the six screws that attach the power supply assembly to the bottom panel; two screws are located in the exhaust air duct, two between the power supply modules, and two between the power supply chassis and the backplane. All six screws must be accessed with a long shaft screwdriver.
4. Remove four screws from the rear panel, one in each corner, and slide the power supply assembly straight out the back.
5. If you are removing the power supply to check the +5 V secondary fuses, stop here. Otherwise, disconnect the wires to the backplane. Note the location of each wire so it can be reconnected to the proper terminal upon reinstallation of the power supply assembly.

Replacement

1. If the wires to the backplane have been disconnected, reconnect them. Refer to Figure 3–1 on page 3–2 for backplane connections. Refer to Figure 5–1 on page 5–2 and Figure 5–2 on page 5–2 for power supply connections.
2. Carefully slide the power supply assembly into the chassis. Make sure that none of the wires interfere with the cooling fan or get pinched between the power supply assembly and the bottom chassis panel.
3. Install and tighten the four screws on the rear panel, one in each corner.
4. Install and tighten the six screws attaching the power supply assembly to the bottom panel.

5. Perform the power supply voltage performance checks described on page 5–1 to verify that the proper voltages are present on the backplane. Make these checks before plugging any cards into the card cage.

Power Supply Module: +5 V, +12 V, and –12 V

WARNING. *To avoid electric shock, allow at least five minutes discharge time after disconnecting primary power before attempting any work on the power supply modules. Many capacitors in the power supply modules retain a substantial charge for several minutes after the power source is disconnected. This charge is present on easily accessible areas, such as heat sinks and capacitor housings.*

WARNING. *To avoid electric shock, use extreme caution when working on the power supply modules while primary power is connected. Voltages up to 660 Volts are always present in the Power Supply Modules while the HFS 9003 is connected to the power source, even when the* ***ON/STANDBY*** *switch is set to standby. These voltages are present on easily accessible areas, such as heat sinks and capacitor housings.*

Removal

1. Follow the procedure for removal of the power supply assembly, described on page 6–5.

2. Remove the two screws from the left edge of the rear panel. The rear panel can now be lowered for access.

3. Mark all the cables connected to the power supply module and disconnect them.

4. Remove the four screws that attach the power supply module metal bracket to the rear panel. Leave the metal bracket attached to the power supply module. Remove the power supply module.

Replacement

1. Position the power supply module in the rear of the power supply assembly, with the primary power connector to the left. Install and tighten four screws attaching the power supply module to the rear panel.

2. Reconnect all the power supply wiring. Refer to Figure 3–1 on page 3–2 for backplane connections. Refer to Figure 5–1 on page 5–2 and Figure 5–2 on page 5–2 for power supply connections.

3. Position the rear panel onto the power supply assembly, then install the two screws along the left edge.

4. Carefully slide the power supply assembly into the chassis. Make sure that none of the wires interfere with the cooling fan or get pinched between the power supply assembly and the bottom chassis panel.
5. Install and tighten the four screws on the rear panel, one in each corner.
6. Install and tighten the six screws attaching the power supply assembly to the bottom panel.
7. Reinstall the top cover of the power supply assembly, installing and tightening the ten screws.
8. Perform the power supply voltage performance checks described on page 5–1 to verify that the proper voltages are present on the backplane. Make these checks before plugging any cards into the card cage.

Power Supply Module: –5.2 V, –2 V, and +24 V

⚠ ***WARNING.*** *To avoid electric shock, allow at least five minutes discharge time after disconnecting primary power before attempting any work on the power supply modules. Many capacitors in the power supply modules retain a substantial charge for several minutes after the power source is disconnected. This charge is present on easily accessible areas, such as heat sinks and capacitor housings.*

⚠ ***WARNING.*** *To avoid electric shock, use extreme caution when working on the power supply modules while primary power is connected. Voltages up to 660 Volts are always present in the Power Supply Modules while the HFS 9003 is connected to the power source, even when the* ***ON/STANDBY*** *switch is set to standby. These voltages are present on easily accessible areas, such as heat sinks and capacitor housings.*

Removal

1. Follow the procedure for removal of the power supply assembly as described on page 6–5.
2. Remove the two screws along the left edge of the power supply assembly rear panel, allowing the rear panel to be lowered.
3. Mark all the cables connected to the power supply module and disconnect them.
4. Remove the four screws attaching the power supply module metal bracket to the front panel of the power supply assembly. Leave the metal bracket attached to the power supply module. Remove the power supply module.

Replacement

1. Position the power supply module in the front of the power supply assembly, with the primary power input connector to the left. Install and tighten four screws attaching the power supply module to the front panel of the power supply assembly.
2. Reconnect all power supply wiring. Refer to Figure 3–1 on page 3–2 for backplane connections. Refer to Figure 5–1 on page 5–2 and Figure 5–2 on page 5–2 for power supply connections.
3. Position the rear panel onto the power supply assembly, then install and tighten the two screws along the left center edge of the rear panel.
4. Carefully slide the power supply assembly into the chassis. Make sure that none of the wires interfere with the cooling fan or get pinched between the power supply assembly and the bottom chassis panel.
5. Install and tighten the four screws on the rear panel, one in each corner.
6. Install and tighten the six screws attaching the power supply assembly to the bottom panel.
7. Reinstall the top cover of the power supply assembly, installing and tightening the four screws.
8. Perform the power supply voltage performance checks described on page 5–1 to verify that the proper voltages are present on the backplane. Make these checks before plugging any cards into the card cage.

Backplane Secondary Fuses

Secondary power fuses are located in inline fuse holders in the +5 V cabling between the power supply module and the backplane. These fuses protect against catastrophic failure, and will not normally blow. The +5 V supply has five fuses, one for each backplane slot. The appropriate fuse should be checked if the +5 V supply to a single slot has failed.

Removal

1. Remove the top cover as described on page 6–4.
2. Remove the power supply assembly as described on page 6–5. *Do not remove the power supply wires from the backplane, which is the last step of that procedure,.*
3. In the +5 V wires between the power supply and the backplane, locate an open the inline fuse holders. There are five of these holders, one for each card slot.

Replacement

1. Replace any faulty secondary fuses with 12 A, 250 V, type 3AG fuses, Tektronix part number 159-0088-00. Install them in the inline fuse holders.
2. Replace the power supply assembly as described on page 6–5.
3. Replace the top cover as described on page 6–4.

Backplane

The backplane is the board that the CPU, time base, and pulse or data generator cards plug into.

Removal

1. Remove the top cover as described on page 6–4.
2. Remove the power supply assembly as described on page 6–5. Perform the last step of that procedure, the removal of power supply wires from the backplane.
3. Remove the fan wires and **ON/STANDBY** switch cables from the front side of the backplane.
4. Remove the twelve screws that attach the backplane to the card cage rear brackets. Lift the backplane out of the mainframe.

Replacement

1. Set the back plane jumpers as shown in Figure 6–2 on page 6–10.
2. Physically place the backplane in its approximate installed position.
3. Connect the fan and **ON/STANDBY** switch cables to the front side of the backplane. Note that the card cage rear bracket has multiple screw holes for the backplane mounting screws. The correct screw holes are those that will position the bottom edge of the backplane $1/16$ inch to $1/8$ inch (2 to 3 mm) above the chassis bottom panel. You can use any HFS 9003 card to align the backplane during installation.
4. Install and tighten the twelve backplane mounting screws. The center two rows of screws have two flat washers under each of the screw heads; the other screws have one flat washer each.
5. Reconnect all power supply wiring. Position the wires carefully so they will not be damaged. Refer to Figure 3–1 on page 3–2 for backplane connections. Refer to Figure 5–1 on page 5–2 and Figure 5–2 on page 5–2 for power supply connections.
6. Perform the power supply voltage performance checks described on page 5–1 to verify that the proper voltages are present on the backplane. Make these checks before plugging any cards into the card cage.

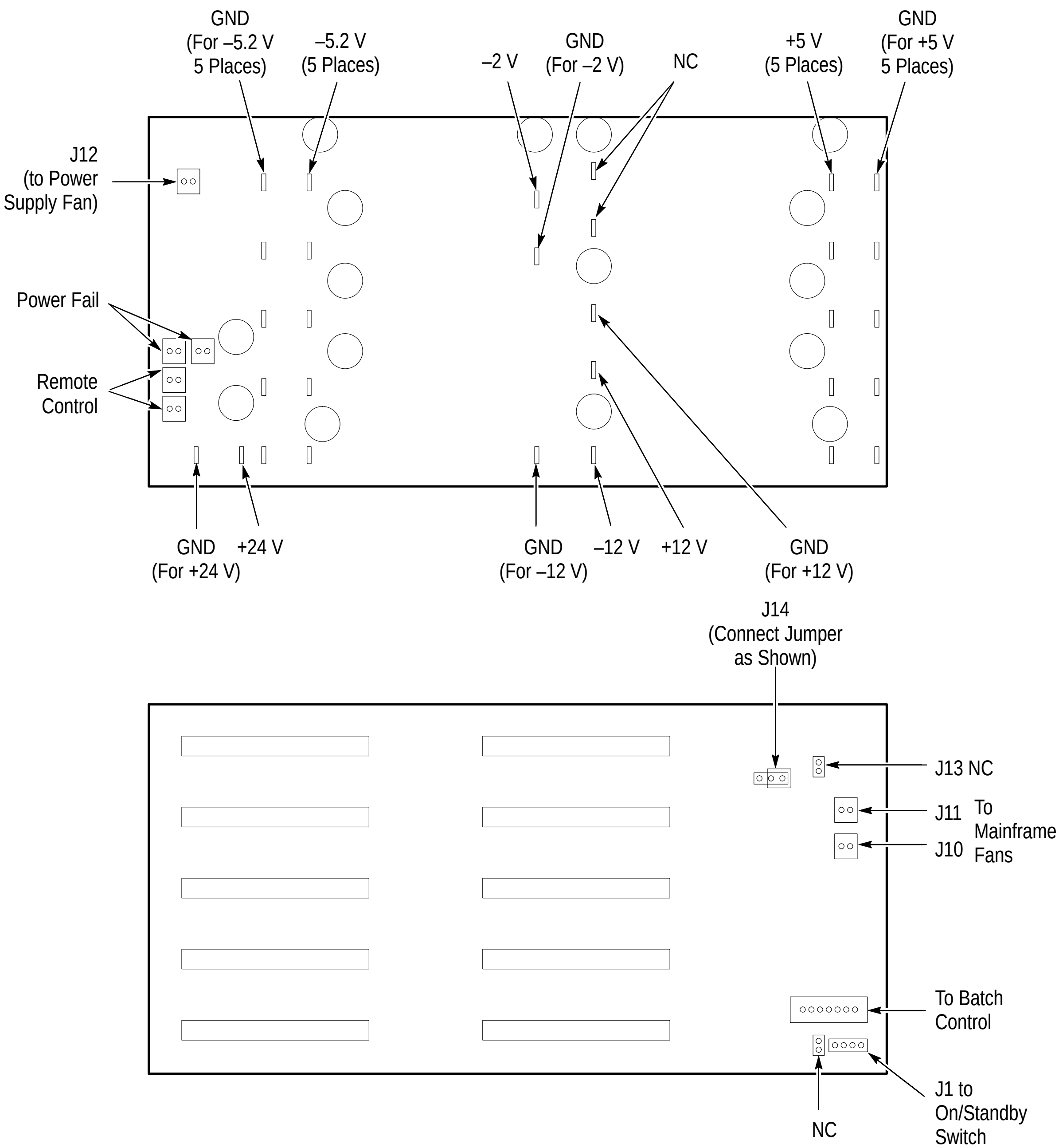


Figure 6–2: Backplane Jumper Settings

Fans

Removal

1. Remove the top cover as described on page 6–4.
2. Use a long shaft screwdriver to remove the six screws that attach the fan bracket to the bottom chassis panel.
3. Remove the two screws that attach the top of the fan bracket to the card cage.
4. Unplug the two fan power connectors from the backplane at J10 and J11.
5. Carefully lift the fan assembly from the chassis, taking care not to entangle the power switch cable in the fan bracket. Remove the screws that attach the fans to the fan bracket.

Replacement

1. Install the fans in the fan bracket.
2. Slide the fan assembly into the mainframe, taking care not to pinch the **ON/STANDBY** switch cable between the fan bracket and the bottom chassis panel.
3. Connect either fan power cable to J10 and the other fan power cable to J11.
4. Using a long shaft screwdriver, install and tighten six screws that attach the fan bracket to the bottom chassis panel.
5. Install and tighten two screws attaching the top of the fan bracket to the card cage.
6. Replace the top cover as described on page 6–4.

ON/STANDBY Lamp

You do not need to remove the **ON/STANDBY** switch to replace its illuminating lamp.

Removal

1. Remove the front panel module as described on page 6–3.
2. Pull the translucent lamp cover straight off the switch. The sides are notched for grasping.
3. Use a lamp puller to remove the lamp.

Replacement

1. Push a replacement lamp (14 V, 80 mA, Tektronix part number 150-0146-00) into the empty lamp holder.
2. Push the translucent lamp cover onto the switch, then press firmly to seat the cover.

3. Replace the front panel module as described on page 6–3.

ON/STANDBY Switch

Removal

1. Remove the front panel module as described on page 6–3.
1. Remove the top cover as described on page 6–4.
2. Disconnect the **ON/STANDBY** switch cable from the backplane at J1.
3. Remove the four screws, one from each corner, from the mainframe front panel (not the front panel module). Loosen the four captive screws around the card cage opening in the front front of the mainframe. Lift out the mainframe front panel.
4. Release the locking tabs that hold the **ON/STANDBY** switch on the front panel, and remove the switch and cable.

Replacement

1. Insert the power switch into the mainframe front panel until the locking tabs snap into position.
2. Thread the **ON/STANDBY** switch cable under the fans to the backplane, and connect them to J1. (It may be easier if you remove the fan bracket to route and connect the cable — see page the Fans Removal procedure on 6–11.)
3. Place the mainframe front panel into position and tighten four captive screws around the card cage opening. Install and tighten the four screws, one in each corner of the mainframe front panel.
4. Replace the top cover as described on page 6–4.
5. Replace the front panel module as described on page 6–3.

Troubleshooting

Most of the troubleshooting information in this section covers the power supplies and mainframes. Card modules are not repairable other than by replacement.

Fuses

Two primary power fuses are located on the rear panel. One fuse supplies power to the +5 V, +12 V, and –12 V power supply module; the other fuse supplies power to the –5.2 V, –2 V, and +24 V power supply module. These fuses should be inspected if voltage checks at the backplane indicate that a group of supply voltages have failed. To remove fuses, insert a screwdriver into the slot of the fuse holder cap, press in, and turn 1/8 turn counterclockwise.

Secondary power fuses are located in inline fuse holders in the +5 V cabling between the power supply module and the backplane. These fuses protect against catastrophic failure, and will not normally blow. The +5 V supply has five fuses, one for each backplane slot. The appropriate fuse should be checked if the +5 V supply to a single slot has failed. To gain access to the fuses, remove the power supply assembly from the mainframe.

Power Supply Modules

If either power supply module detects a power interruption or other failure, it may shut off both itself and the other power supply module. This shutdown, accomplished through the **REMOTE SENSE** lines, prevents card module damage due to partial power on conditions.

To determine which power supply module is forcing shutdown, disable the **REMOTE CONTROL** function.

CAUTION. *To avoid damaging the card modules, remove all the cards before the performing the following procedure.*

Disconnect the **REMOTE CONTROL** line from both power supply modules. These lines are single small-gauge wires that attach to the power supply main circuit boards. They can be identified by the connector that is installed in the line, specifically for this test.

After disconnecting the **REMOTE CONTROL** line, apply power and perform the power supply voltage check procedure on page 5–1. Reconnect the **RE-**

MOTE CONTROL lines after performing the check and making necessary repairs.

Electrical Noise

Unlike many high efficiency switching supplies, the HFS 9003 power supply modules are designed to provide low noise power from no-load to full-load conditions. If a performance check indicates excessive electrical noise, environmental conditions or measurement technique should be inspected first.

Extremely noisy primary power can cause noisy DC voltages. An oscilloscope can be used to check incoming primary power. If excessive noise is found, an external line filter can be installed.

Faulty card modules can cause the power supplies to appear noisy. To check, remove the card modules from the mainframe and test the supplies again for noise.

When measuring noise, establish a good ground for the oscilloscope probe. Use as short a probe ground lead as possible. Connect the probe ground lead to one of the backplane ground lugs, not the chassis. Use the oscilloscope bandwidth limit since noise above 10 MHz does not indicate a problem.

Occasionally a defective cooling fan can inject noise into the +12 V supply even though the fan appears to be operating normally. To check this, unplug the fan power cables one at a time while monitoring the +12 V supply with an oscilloscope. This check should be performed twice: first with backplane jumper J13 installed; second with J13 removed, J14 in the low speed position, and the thermistor chilled to operate the fans at their lowest operating speed.

If noise appears on the –5.2 V, –2 V, or +24 V supplies, connect a 5 Ω to 10 Ω resistor to the –5.2 V supply. If the noise disappears, no problem is indicated because the noise is present only when the supply is unloaded. That does not affect normal operation of these power supplies.

Loose screws or loose covers can cause an increase in radiated EMI.

Fans

There are two circuits controlling the fans. One circuit controls the power supply module cooling fan, the other controls the two card cage fans. Both circuits are located on the backplane, and both use the same temperature sensor. All three fans draw power from the +12 V power supply. None of the fans may run if the mainframe is very cold. The fans normally start running after several minutes of operation.

The card cage fans are controlled by two user-configurable jumpers. They may run continuously at full speed, or at one of two variable speed ranges. These fans should be running at some speed whenever the **ON/STANDBY** switch is on and the mainframe is at or above room temperature. If one fan does not run, then the fan and cabling should be inspected. If both fans fail to run, the backplane circuitry may have failed.

The power supply module cooling fan always runs at a variable rate, and the variability is not user-configurable. It should always be running at some speed when the **ON/STANDBY** switch is on and the mainframe is at or above room temperature. If the fan is not running, temporarily move its power cable from J12 on the rear of the backplane to J11 on the front of the backplane. If the fan then functions, the backplane circuitry may have failed. If the fan still does not run, either the fan or its cable has failed.

If none of the fans are running, verify that the +12 V supply is operational. Check that the thermistor is not damaged. Check the thermistor by attaching a jumper across its leads; if the fans then run, the thermistor has failed. If the fans can be made to run by reconfiguring the two fan control jumpers, a backplane circuit failure is indicated.

Backplane Connectors

If a backplane card connector is suspect, a continuity check can be made using a digital multimeter (DMM) and a length of 22 AWG copper wire. This gauge wire will not damage the VXIbus module connector sockets, and can be used as a probe. The copper wire probe can also be used for checking voltages directly at the connector instead of at the through-hole power lug test points. If you find a bad backplane card connector, replace the backplane. The backplane card connectors are press fit into the backplane and cannot be replaced.

Diagnostics

This section provides information necessary to troubleshoot the HFS 9003 at the circuit board level. The primary troubleshooting method is to use the power-on and self-test diagnostics to identify faulty Field Replaceable Units (FRUs). The FRUs include the plug-in cards, front panel module, power supply units, fans, knobs, switches, and any individual component that is listed in the *Mechanical Parts List* section of this manual.

Power-On Diagnostics

Power-on diagnostics execute automatically whenever the mainframe power is switched on. The HFS 9003 uses three stages of diagnostics: kernel test, controller test, and self test, which run consecutively. Diagnostics advance to the next stage only if the preceding stage does not detect an error. In self-test diagnostics, once an error message is displayed on the screen you can request that the diagnostics continue. When all tests successfully complete, the instrument goes into normal operating mode. Test failures result in error code outputs which can be cross-referenced to suspect FRUs.

Kernel-Test Diagnostics

The kernel test is the first stage of diagnostics. It verifies the functionality of the hardware needed to run the internal operating system.

Controller-Test Diagnostics

The controller test is the second stage of diagnostics. It is run by the internal operating system. It verifies the CPU support circuitry on the controller (CPU) card, the backplane bus, and the front panel module.

Self-Test Diagnostics

The self test is the last stage of diagnostics and verifies the functionality of the time base card and the pulse or data generator cards. This test differs from the kernel- and controller-test diagnostics in two ways. First, the self-test diagnostics display messages on the screen. Once a self-test failure has occurred, you can display more information or continue running the remaining diagnostics.

Second, the self-test diagnostics can be run at any time. Use the Cal/Deskew menu **Self Test** item on the front panel or execute the `*TST?` command from the GPIB or RS-232-C programmable ASCII interface. Refer to the Self-Test Diagnostics Section on page 6–18 of this manual or the *HFS 9000 User Manual* for more information.

Self-Test Diagnostics

You can run the self-test diagnostics using the **Self Test** item in the Cal/Deskew menu. In addition, the same function can be initiated from either ASCII interface (RS-232-C or GPIB) under the control of a remote computer or controller. Refer to the *HFS 9000 User Manual* for detailed information about using the programming interfaces. The `*TST?` query runs the self test and reports the results. The self test does not require operator interaction and does not create bus conditions that violate IEEE 488.1/488.2 standards. When complete, the HFS 9003 returns to the state it was in prior to the self test.

The test response is a value as described in Table 6–1.

Table 6–1: Results from *TST?

Test Response Value	Meaning
0	test completed with no errors detected
SSCC	system which slot and card produced the first detected error: SS = slot number: 01 = CPU slot 02 = time base slot 03 = slot A 04 = slot B . . . CC = card type: 10 = CPU card 20 = time base card 31 = High Speed pulse generator card 32 = Var Rate pulse generator card 33 = High Speed data time generator card 34 = Var Rate data time generator card
9900	system configuration is not valid

The self-test query can take 30 seconds or more to respond. If an error is detected, self test stops and returns that error code, and does not complete any remaining tests.

Calibration

Calibration measures the performance of the HFS 9003 against specifications, and performs automatic internal adjustments to bring the HFS 9003 into specification. This is different from the diagnostics, which only verify that the circuits are operational.

Calibration is normally a function initiated by the user. However, calibration can be automatically initiated by the power-on diagnostics if they determine that the HFS 9003 is out of specification or has been reconfigured.

It is possible to generate error codes by running a calibration procedure at some time other than power on.

Error Indications

There are two mechanisms for reporting errors: diagnostic LED error indexes and extended mode menus.

Kernel-test and controller-test failures are identified by a LED error index, and, if they are not display related, by a displayed error message. These messages are of the following form:

CONTROLLER DIAGNOSTICS FAILED <test name>

When any kernel test or controller test fails, the CPU hangs in a loop and the instrument appears dead. For corrective action, see Table 6–2 and Figure 6–5.

Kernel and controller testing occurs quickly, so the LEDs will only turn on briefly as they switch between on and off states. If the LEDs never turn on during power on, or if any LEDs remain lit, then an error is indicated.

Self-test errors are identified by LED error indexes that indicate the faulty card, and also by extended mode menus on the front panel. In all cases, a faulty FRU is identified by the LED error indications.

Bit Assignments For Diagnostic LEDs

The bank of diagnostic LEDs is located on the CPU card inside the LED cover. Figure 6–3 shows the location of the LED cover and LEDs. To see the LEDs, remove the LED cover by removing the screw. A firmware update stick might be installed in the slot behind the cover. You can see a bank of eight LEDs on the side nearest to the serial port connector. You may need to use a small flashlight to see all the unlit LEDs.

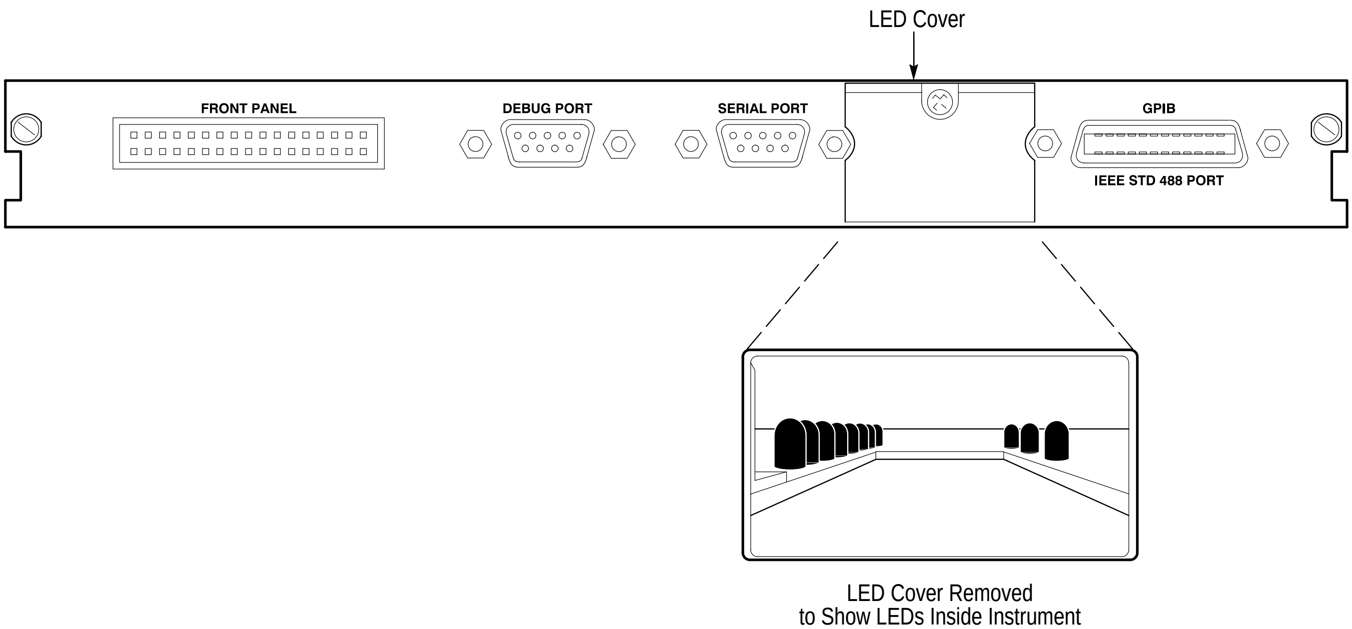


Figure 6–3: The Location of LEDs on the CPU Card

The eight LEDs are numbered D6 (farthest from the front panel) through D13 (nearest the front panel), as shown in Figure 6–4.

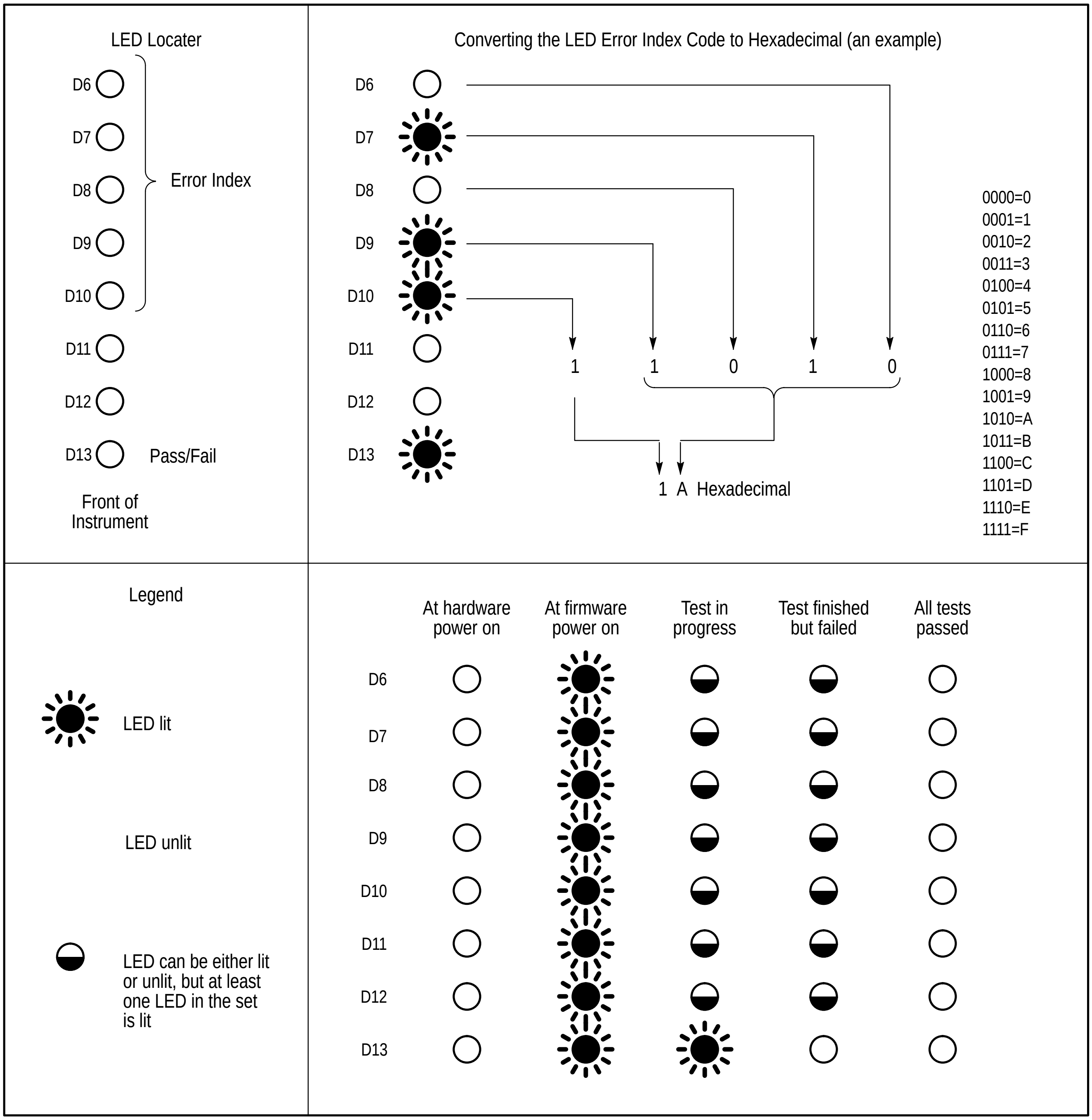


Figure 6–4: Bit Assignments for Diagnostic LEDs

The onset, completion, or failure of testing is indicated by LED D13. The five lowest LEDs, D6 through D10, combine to display the error index code. In the discussions below, these five LEDs are combined to make a hexadecimal value in the range of 00 through 1F. LED D6 is the low order bit, and LED D10 is the high order bit.

At power on, status LEDs are turned off. At the start of the tests, status LEDs are turned on. If a kernel test fails but completes execution, the D13 LED turns off and the processor stops. If a kernel test is unable to finish, The D13 LED remains lit. To identify a failed test, read the error index code.

Diagnostic Procedure

Table 6–2 and Figure 6–5 indicate how to proceed from each of the error index codes. Codes 1B and higher provide a message on the screen. You can press any button other than **SELECT** to see additional error information. This can be easier than decoding the error index code.

Table 6–2: Troubleshooting From the Error Index Code

If you see this Error Index Code[1]	Do This
01 through 09, 0B through 0F, 11	Replace CPU card.
0A	Replace front panel module and cable.
10	Follow the diagnostic procedure flowchart (Figure 6–5) at step A.
1A	Remove cards one by one and retest; always remove cards from the top down, and stop before removing the CPU card. When you remove the last pulse or data generator card, you will observe a configuration error (1B); ignore it and press **SELECT** to continue. If the test passes, the last card removed is faulty. If the 1A failure persists when only the CPU card is installed, then the possible sources of trouble are the CPU card or the backplane.
1B	Make sure the CPU card is installed in the lowest card slot, the Time Base card is installed in the next to lowest card slot, and the pulse or data generator cards are installed immediately above. Any unused card slots must be at the top. If these conditions are met and the error persists, follow the procedure for Error Index Code 1A.
1E	Check clock distribution cables (see Figure 6–1 on page 6–4). If correct, follow the diagnostic procedure flowchart (Figure 6–5) at step B.
1F	Replace time base card.

1 **These values are hexadecimal.**

***NOTE**. If you observe multiple error messages, verify the power supply voltages before proceeding. Marginal power supply voltages can cause other apparently unrelated failures. See the Adjustment Procedures section for information on verifying and adjusting power supplies.*

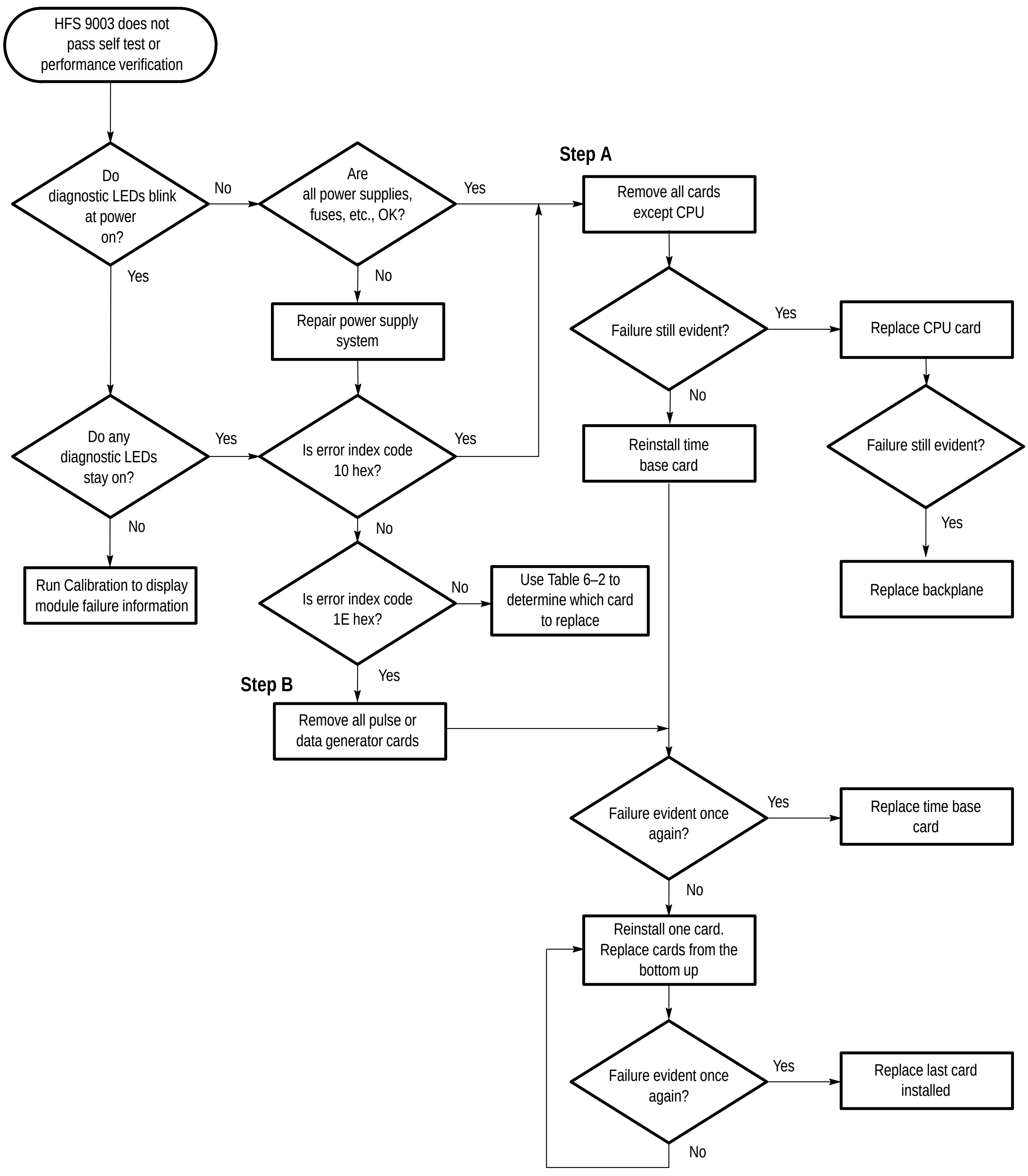


Figure 6–5: Diagnostic Procedure Flowchart

Options

The HFS 9003 is configured at the factory with the number and types of pulse or data generator cards specified at the time of ordering. Additional pulse and data generator cards can be installed if your HFS 9003 has available slots. Refer to the *Mechanical Parts List* section of this manual for part numbers and ordering information.

Installation should be performed by qualified service personnel. After installation, you should calibrate the HFS 9003 (refer to the *HFS 9000 User Manual* for Calibration procedures). You should also run the Performance Verification procedures in this manual to ensure proper operation.

Electrical Parts List

Refer to the *Mechanical Parts List* section of this manual for a list of all parts.

Block Diagram

The HFS 9003 consists of three major electrical sections: mainframe, front panel, and cards. Six types of cards may be installed in the HFS 9003:

- CPU card
- Time base card
- High speed pulse generator card (HFS 9PG1)
- Variable rate pulse generator card (HFS 9PG2)
- High speed data generator card (HFS 9DG1)
- Variable rate data generator card (HFS 9DG2)

Each HFS 9003 must have one CPU card, one time base card, and at least one generator card. Figure 9–1 shows how these modules are interconnected.

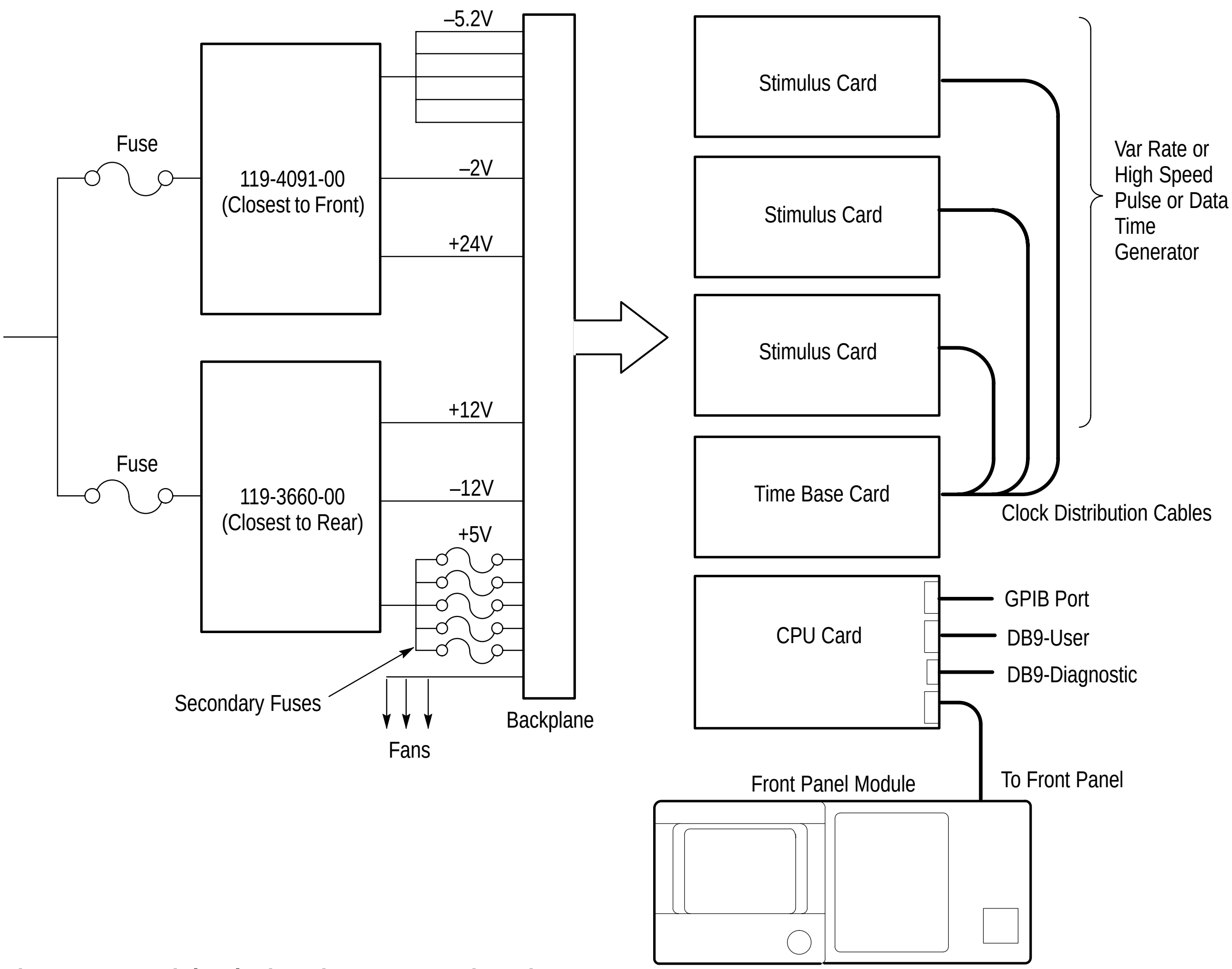


Figure 9–1: Module Block and Interconnection Diagram

Replaceable Parts List

This section contains a list of the components that are replaceable for the HFS 9003. As described below, use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. service center or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If a part you order has been replaced with a different or improved part, your local Tektronix service center or representative will contact you concerning any change in the part number.

Change information, if any, is located at the rear of this manual.

Module Replacement

The HFS 9003 is serviced by module replacement so there are three options you should consider:

- **Module Exchange.** In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEKWIDE, ext. BVJ5799.
- **Module Repair.** You may ship your module to us for repair, after which we will return it to you.
- **New Modules.** You may purchase new replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find the all the information you need for ordering replacement parts.

Item Names

In the Replaceable Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, U.S. Federal Cataloging Handbook H6–1 can be used where possible.

Indentation System

This parts list is indented to show the relationship between items. The following example is of the indentation system used in the Description column:

1 2 3 4 5 Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
(END ATTACHING PARTS)
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
(END ATTACHING PARTS)
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
(END ATTACHING PARTS)

Attaching parts always appear at the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. Attaching parts must be purchased separately, unless otherwise specified.

Abbreviations

Abbreviations conform to American National Standards Institute (ANSI) standard Y1.1

CROSS INDEX – MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S3109	FELLER	72 VERONICA AVE UNIT 4	SUMMERSET NJ 08873
TK0413	ADAMS SUPPLY COMPANY	1850 W 205TH ST PO BOX 2938	TORRANCE CA 90509
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609–3320
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1374	TRI–TEC ENGINEERING CORP		
TK1499	AMLAN INC	97 THORNWOOD RD	STAMFORD CT 06903–2617
TK2359	STROM	5289 NE ELAM YOUNG PARKWAY SUITE E 300	HILLSBORO OR 97124
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE #2	VANCOUVER WA 98601
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661–2999
0J260	COMTEK MANUFACTURING OF OREGON (METALS)	PO BOX 4200	BEAVERTON OR 97076–4200
0KB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
05006	20TH CENTURY PLASTICS INC	3628 CRENSHAW BLVD PO BOX 30231	LOS ANGELES CA 90030
06383	PANDUIT CORP	17301 RIDGELAND	TINLEY PARK IL 07094–2917
08806	GENERAL ELECTRIC CO MINIATURE LAMP PRODUCTS DEPT LIGHTING BUSINESS GROUP	NELA PK	CLEVELAND OH 44112
11897	PLASTIGLIDE MFG CORP	2701 W EL SEGUNDO BLVD	HAWTHORNE CA 90250–3318
2K262	BOYD CORP	6136 NE 87TH AVE PO BOX 20038	PORTLAND OR 97220
29870	VICTOR CORP	618 MAIN STREET	WEST WARWICK RI 02893
50463	POWER SYSTEMS INC.	45 GRIFIN ROAD	SOUTH LINFIELD, CT 06002
61857	SAN–0 INDUSTRIAL CORP	85 ORVILLE DR PO BOX 511	BOHEMIA LONG ISLAND NY 11716–2501
62559	SCHROFF INC	170 COMMERCE DR	WARWICK RI 02886–2430
75915	LITTELFUSE INC SUB TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016–3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001
81041	HOWARD INDUSTRIES DIV OF MSL INDUSTRIES INC	1 NORTH DIXIE HWY PO BOX 287	MILFORD IL 60953
91836	KINGS ELECTRONICS CO INC	40 MARBLEDALE ROAD	TUCKAHOE NY 10707–3420

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
8–1–1	672–1393–02	B010411		1	CIRCUIT BD ASSY:HUMAN INTFC,BEZEL,LWR/TOP PNL	80009	672139302
–2	213–1035–00			4	SCREW,MACHINE:M2.5 X 11,COLLAR,SST,NI PL	62559	21100–379
–3	213–0183–00			4	SCREW,TPG.TF:6–2– X 0.5,TYPE B,STL	TK0435	ORDER BY DESC
–4	407–4070–00			1	BRACKET,FR PNL:HOLDING,LEFT,SST	80009	407407000
–5	333–3776–00			1	PANEL,FRONT: ,LEXAN ON AL	80009	333377600
–6	166–0670–00			4	SLV,INSUL,ELEC:PLASTIC,GRAY,0.23	62559	21100–464
–7	213–0192–00			4	SCREW,TPG,TF:6–32 X 0.5,SPCL TYPE,FILH,STL	TK0435	8887–312
–8	211–0504–00			6	SCREW,MACHINE:6–32 X 0.250,PNH,STL	TK0435	ORDER BY DESC
–9	381–0473–00			8	NUT BAR:THREADED INSERT,6.18 L,AL	62559	30819–648
–10	426–2365–00			1	FRAME,CABINET:	80009	426236500
–11	386–6002–01			2	PLATE,FRONT:SLOT COVER,AL	80009	386600201
–12	262–1034–00			1	SWITCH ASSY:SPST W/LIGHT,CONDUCTOR,22AWG,14.5 L	80009	262103400
–13	407–3680–00			1	BRACKET,FR PNL:HOLDING,RIGHT,SST	80009	407368000
–14	212–0008–00			2	SCREW,MACHINE:8–32 X 0.5,PNH,STL CD PL	TK0435	ORDER BY DESC
–15	366–0582–01			1	KNOB:ENCODER	TK1163	ORDER BY DESC

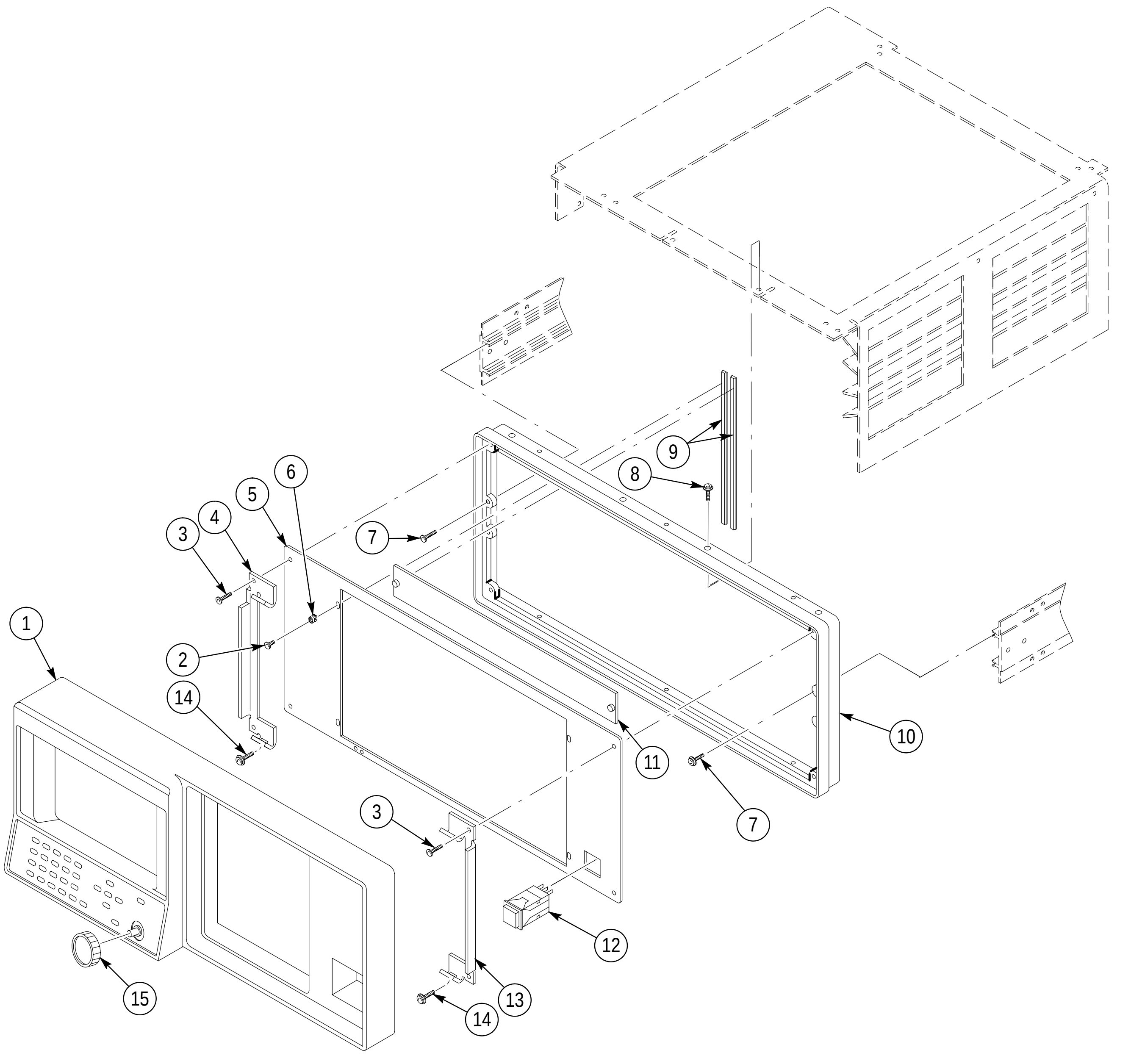


Figure 10–1: Front Panel

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
8–2–1	337–3631–01			1	SHIELD,ELEC:POWER SUPPLY,AL	80009	337363101
–2	211–0658–00			16	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ	TK0435	17691–300
–3	426–2365–00			1	FRAME,CABINET:	80009	426236500
–4	213–0192–00			4	SCREW,TPG,TF:6–32 X 0.5,SPCL TYPE,FILH,STL	TK0435	8887–312
–5	333–3777–00			1	PANEL,REAR:AL	80009	333377700
–6	343–0549–00			7	STRAP,TIEDOWN,E:0.098 W X 4.0 L,ZYTEL	TK1499	HW–047
–7	352–0787–00			2	FUSEHOLDER:3AG,20A,250V W/CAP & CARRIER	75915	3453LS3N
–8	213–0146–00			4	SCREW,TPG,TF:6–20 X 0.312,TYPE B,PNH,STL	TK0435	ORDER BY DESC
–9	352–0482–00			1	HOLDER,CA TIE:0.75 SQ,STICKY BACK,PLASTIC	06383	ABMM–AT–D
–10	119–3660–00			1	POWER SUPPLY:SWITCHING	80009	119366000
–11	119–4091–00			1	POWER SUPPLY:SWITCHING,AUTO IN 85–264 VAC	50463	PSI 175X–108
–12	441–1941–00			1	CHAS,PWR SUPPLY:ALUMINUM	80009	441194100
–13	358–0215–00			1	GROMMET,PLASTIC:BLACK,U–SHAPED,0.524ID	80009	358021500
–14	671–1650–01			1	CIRCUIT BD ASSY:POWER MONITOR	80009	671165001
–15	211–0504–00			8	SCREW,MACHINE:6–32 X 0.250,PNH,STL	TK0435	ORDER BY DESC
–16	255–0334–00			1	PLASTIC CHANNEL:12.75 X 0.175 X 0.155,NYLON	11897	122–NN–2500–060
–17	211–0510–00			4	SCREW,MACHINE:6–32 X 0.375,PNH,STL CD PL	TK0435	ORDER BY DESC

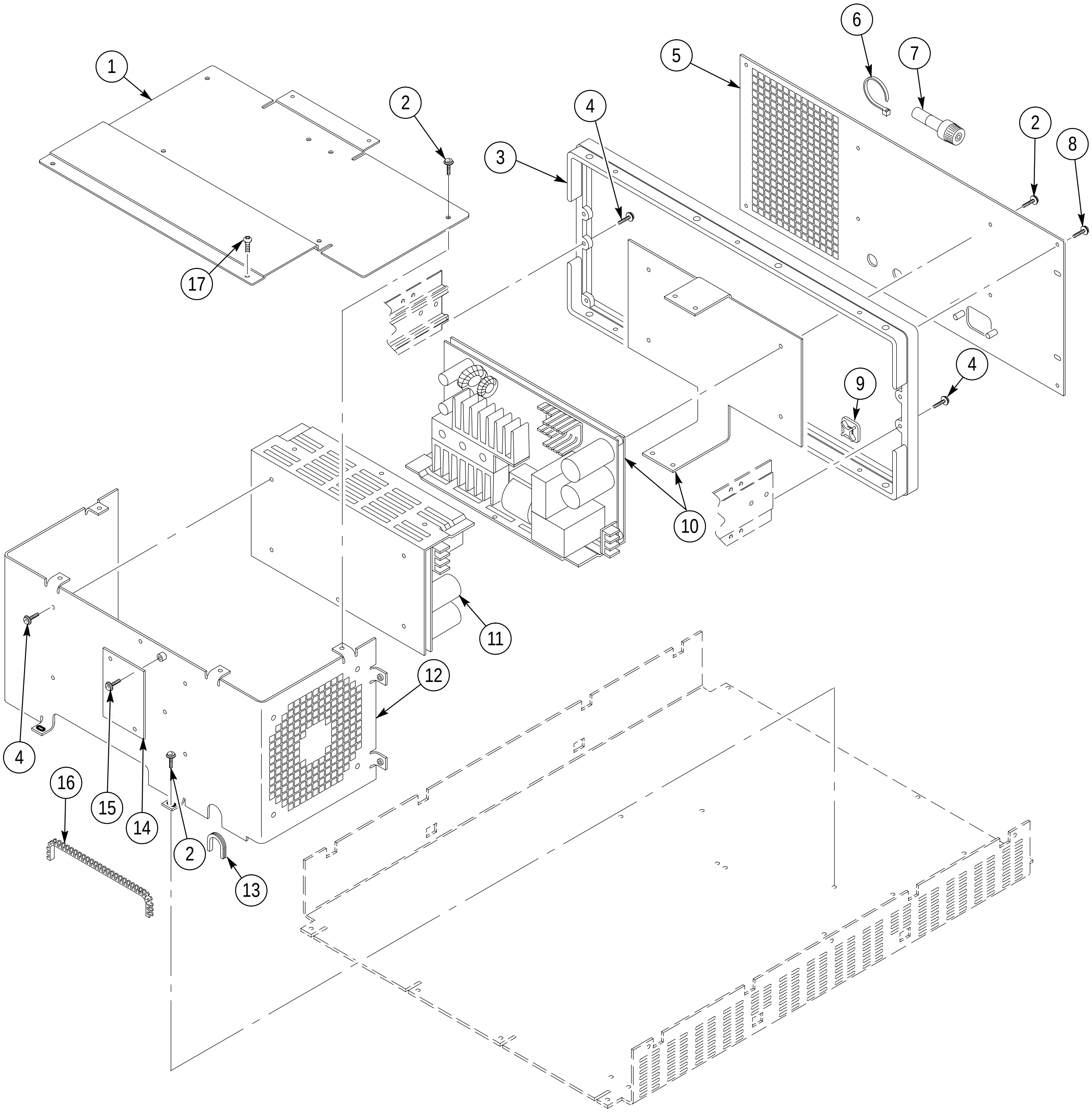


Figure 10–2: Rear Panel and Power Supply

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
8–3–1	211–0474–00			12	SCREW,MACHINE:M5 X 12 FH,STL,PHILLIPS POZIDRIVE	0KB01	211–0474–00
–2	426–2367–00			2	RAIL,REAR:ALUMINUM,6.2 L	62559	30837–565
–3	342–0901–00			4	INSULATOR,STRIP:6.076 L,PLASTIC	62559	33890–289
	343–1247–00			8	CLIP,RETAINER:PLASTIC,INSULATING STRIP	80009	343124700
–4	671–1981–02			1	CIRCUIT BD ASSY:BACK PLANE BOARD	80009	671198102
–5	213–1036–00			12	SCREW,MACHINE:M2.5 X 10,CHEESE HD,STL	62559	21100–138
–6	210–0938–00			18	WASHER,FLAT:0.109 ID X 0.25 OD X 0.32	TK0413	ORDER BY DESC
–7	407–3900–00			1	BRKT,FAN,LEFT:ALUMINUM	80009	407390000
	378–0377–00			1	SCREEN,FAN:4.8 SQ,SST	80009	378037700
	200–2222–00			3	GUARD,FAN	81041	6–182–033
–8	119–2421–01			3	FAN,TUBEAXIAL:12VDC,7.1V,3680RPM,102CFM W/CONN	80009	119242101
–9	211–0553–00			8	SCREW,MACHINE:6–32 X 1.5,PNH,STL CD PL	TK0435	ORDER BY DESC
	211–0530–00			4	SCREW,MACHINE:6–32 X 1.750,PNH,STL	TK0435	ORDER BY DESC
	210–0457–00			4	NUT,PL,ASSEM,WA:6–32 X 0.312,STL CD PL	TK0435	ORDER BY DESC
–10	211–0658–00			5	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ	TK0435	17691–300
–11	351–0865–00			10	GUIDE,CKT BD:10.7 L,ALUMINUM	62559	20897–409
–12	386–5961–00			16	SPRT,CKT GUIDE:VX1500 MAINFRAME	0JR05	ORDER BY DESC
–13	386–6010–00			4	SPRT,CKT GUIDE:	80009	386601000
–14	672–1356–02			1	CIRCUIT BD ASSY:VAR RATE PULSE CARD W/FR PANEL	80009	672135602
	672–1355–00			1	CIRCUIT BD ASSY:HI–SPEED PULSE CARD W/FR PANEL	80009	672135500
	671–2454–01	B010100	B010667	1	CIRCUIT BD ASSY:CMOS DATA GEN PULSE CARD W/FP	80009	671245401
	671–4467–00	B010668		1	CIRCUIT BD ASSY:CMOS DATA GEN	80009	671446700
	671–2453–00	B010100	B010130	1	CIRCUIT BD ASSY:ECL HIGH SPEED PULSE CARD W/FP	80009	671245300
	671–2453–01	B010131	B010164	1	CIRCUIT BD ASSY:ECL HIGH SPEED PULSE CARD W/FP	80009	671245301
	671–2453–02	B010165	B010667	1	CIRCUIT BD ASSY:ECL HIGH SPEED PULSE CARD W/FP	80009	671245302
	671–4452–00	B010668			CIRCUIT BD ASSY:ACQ–EXP	8009	671445200
–15	672–0316–01			1	CIRCUIT BD ASSY:TIMEBASE W/FRONT PANEL	80009	672031601
–16	671–2581–01	B010100	B010164	1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258101
	671–2581–02	B010165	B010215	1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258102
	671–2581–04	B010216	B020153	1‘	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258104
	671–2581–05	B020154		1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258105
–17	012–1363–00			1	CABLE ASSY:COMOSITE,2 SHLD,TW PR,6 IN,100OHM	80009	012136300
–18	426–2366–00			2	RAIL,FRONT:ALUMINUM,6.2 L	TK2359	426–2366–00

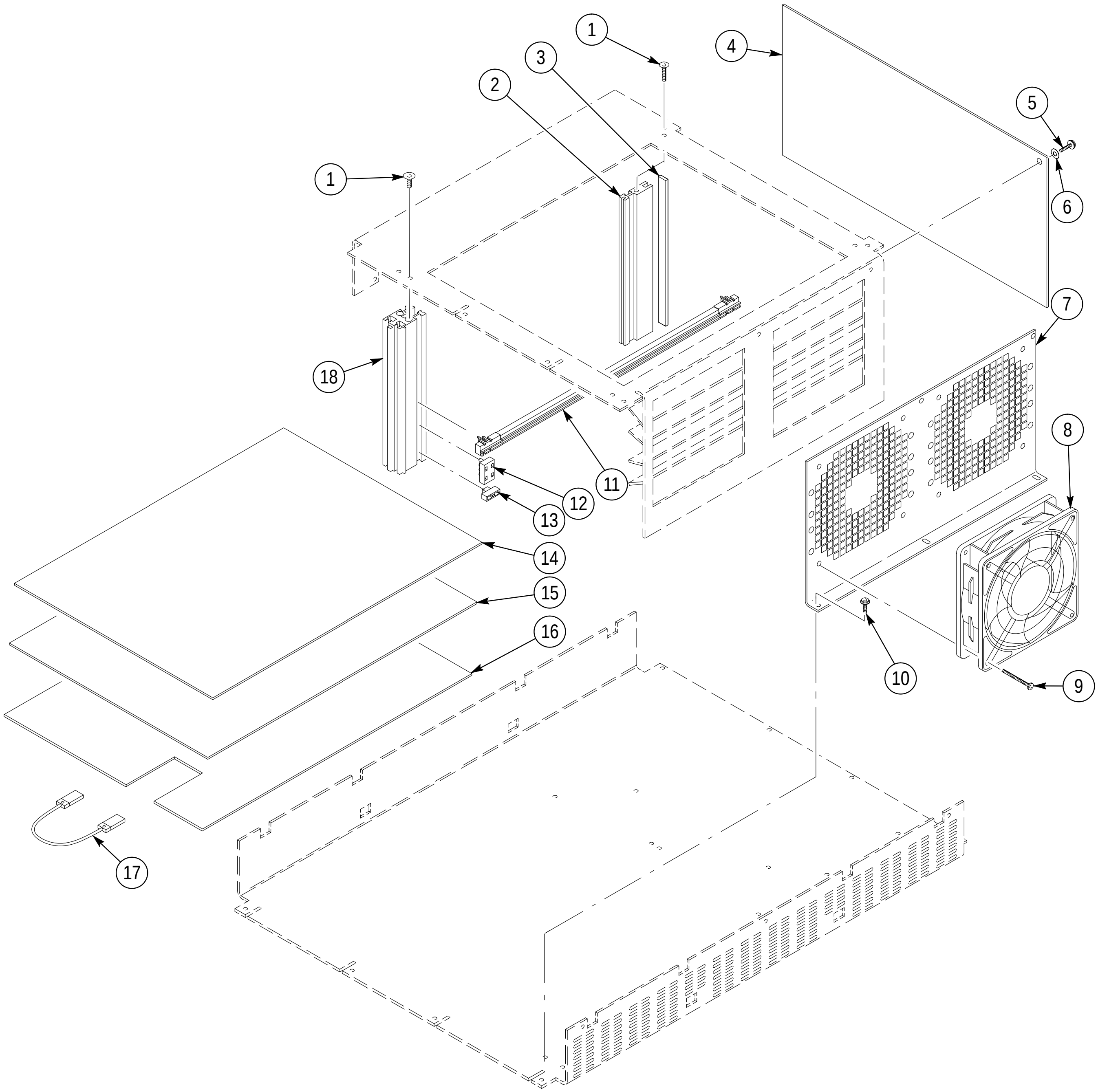


Figure 10–3: Circuit Boards and Fan Assembly

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
8–4–1	211–0101–00			28	SCREW,MACHINE:4–40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESC
–2	390–1086–01			1	CABINET,TOP:ALUMINUM	80009	390108601
–3	213–0192–00			4	SCREW,TPG,TF:6–32 X 0.5,SPCL TYPE,FILH,STL	TK0435	8887–312
–4	407–3921–00			1	BRKT,CHASSIS:ALUMINUM	80009	407392100
–5	426–2368–00			1	RAIL,BACK PLANE:ALUMINUM,6.2 L	62559	426–2368–00
–6	211–0474–00			4	SCREW,MACHINE:M5 X 12 FH,STL,PHILLIPS/POZIDRIVE	0KB01	211–0474–00
–7	441–1939–00			1	CHASSIS,MAIN:ALUMINUM	80009	441193900
–8	386–6000–01			1	RAIL,CABINET:SIDE,RIGHT,AL	80009	386600000
–9	211–0504–00			13	SCREW,MACHINE:6–32 X 0.250,PNH,STL	TK0435	ORDER BY DESC
–10	390–1087–01			1	CABINET,BOTTOM:ALUMINUM	80009	390108700
–11	348–0187–00			4	FOOT,CABINET:BLACK POLYURETHANE	0JR05	ORDER BY DESC
	348–0430–00			1	BUMPER,PLASTIC:BLACK POLYURETHANE	2K262	ORDER BY DESC
–12	348–0080–01			5	FOOT,CABINET:CHARCOAL GRAY,POLYURETHANE	0JR05	ORDER BY DESC
–13	212–0023–00			4	SCREW,MACHINE:4–40 X 0.75,PNH,STL	TK0435	ORDER BY DESC
–14	348–1166–00			2	FOOT,CABINET:BLACK,ANODIZED	80009	348116600
–15	211–0541–00			8	SCREW,MACHINE:6–32 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESC
–16	386–6001–01			1	RAIL,CABINET:SIDE,LEFT,AL	80009	386600101
–17	441–1940–00			1	CHASSIS,TOP:ALUMINUM	80009	441194000
–18	367–0248–07			1	HANDLE,CARRYING:16.34 L,W/CLIP,PLASTIC	0J260	ORDER BY DESC
–19	200–2191–03			2	CAP,RETAINER:PLASTIC	80009	200219103

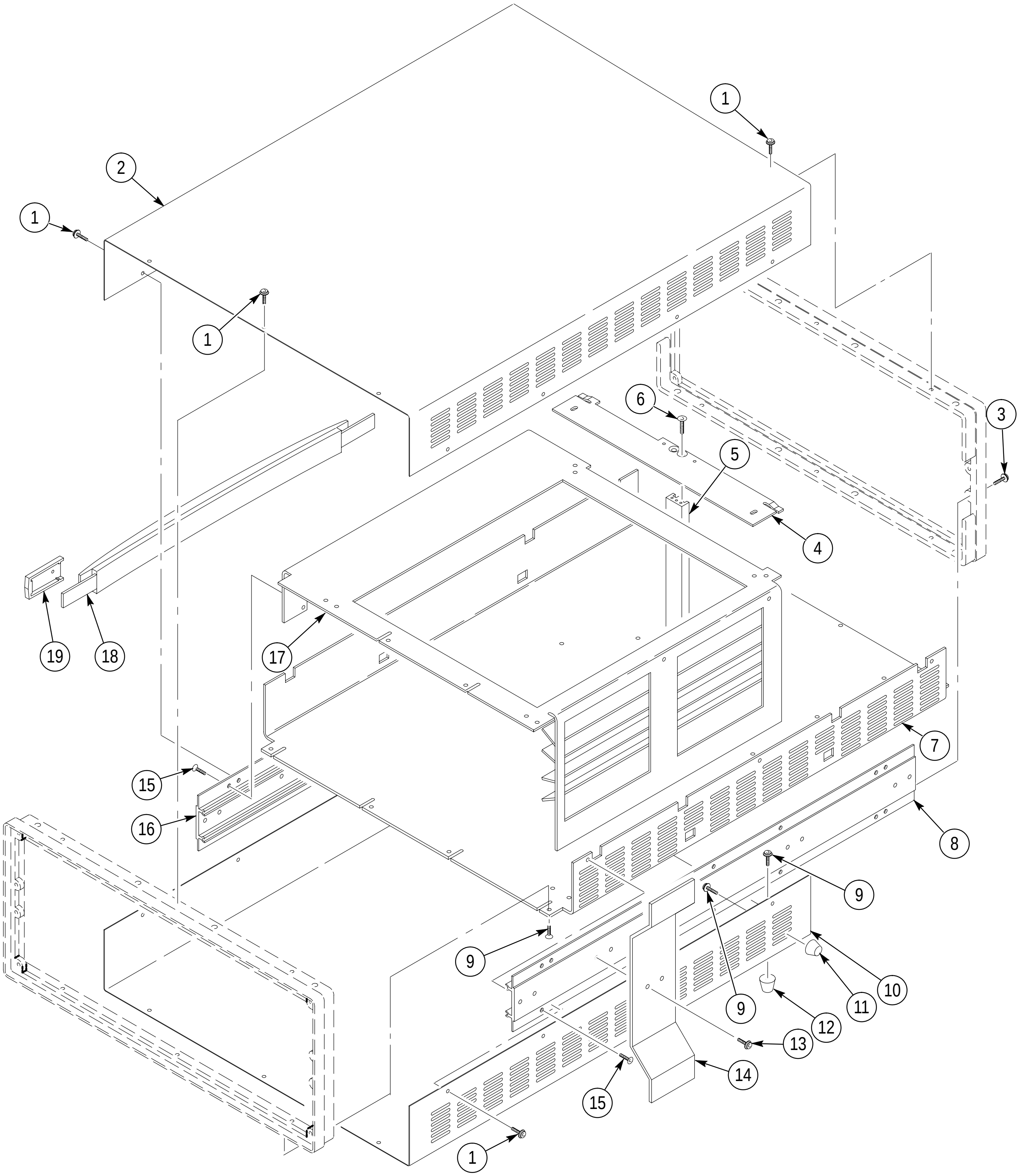


Figure 10–4: Chassis and Covers

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
					ELECTRICAL PARTS		
	150–0146–00			1	LAMP,INCAND:14V,80MA,73E,WEDGE BASE	08806	73E
	159–0088–00			5	FUSE,CARTRIDGE:3AG,12A,250V,6 SEC,CER	75915	314012
					STANDARD ACCESSORIES		
	012–1241–00			1	CABLE ASSEMBLY:RS–232,;180.0 L,9,26 AWG	TK1374	012–1241–00
	015–0572–00			1	ADAPTER,CONN:SMA FEMALE TO BNC MALE	91836	879–4–15–MA9
	016–0537–00			1	POUCH,ACCESSORY:6 IN X 9 IN W/ZIPPER	05006	ZIP–6X9ID
	070–8365–01			1	MANUAL,TECH:USERS,HFS9000 SERIES	80009	070836501
	070–8564–00			1	MANUAL,TECH:SERVICE,HFS 9003	80009	070856400
	159–0014–00			1	FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC	61857	SS2–5A
	159–0017–00			1	FUSE,CARTRIDGE:3AG,4A,250V,FAST BLOW	75915	312 004
	161–0066–00			1	CABLE ASSY,PWR,:3,18AWG,115V,98.0 L (STANDARD)	0B445	ECM–161–0066–00
	161–0066–09			1	CABLE ASSY,PWR,:3,0.75MM SQ,220V,99.0 L (OPTION A1 ONLY–EUROPEAN)	S3109	86511000
	161–0066–10			1	CABLE ASSY,PWR,:THREE 0.75MM SQ,250V,2.5 M (OPTION A2 ONLY–UNITED KINGDOM)	S3109	BS/13–H05VVF3G0
	161–0066–11			1	CABLE ASSY,PWR,:3,0.75MM,240V,96.0 L (OPTION A3 ONLY–AUSTRALIA)	S3109	SAA/3–OD3CCFC3X
	161–0066–12			1	CABLE ASSY,PWR,:3,18 AWG,250V,99.0 L (OPTION A4 ONLY–NORTH AMERICAN)	29870	ORDER BY DESC
	161–0154–00			1	CABLE ASSY,PWR,:3,1.00MM SQ,250V,10A,2.5M (OPTION A5 ONLY–SWITZERLAND)	S3109	12–H05VVF3G 00–
	174–1427–00			1	CABLE ASSY,RF:50 OHM COAX,20.0 LW/BLACK VINYL	TK2469	ORDER BY DESC
					OPTIONAL ACCESSORIES		
	020–1828–00			1	COMPONENT KIT:STANDARD RACKMOUNT	80009	020182800